

## FEATURES

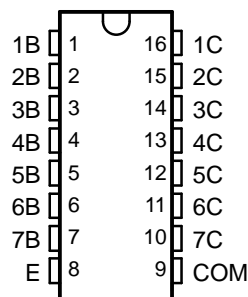
- **500-mA-Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay-Driver Applications**

## DESCRIPTION/ORDERING INFORMATION

The ULN2003AI is a high-voltage, high-current Darlington transistor array. This device consists of seven npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

The ULN2003AI has a 2.7-k $\Omega$  series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

**D, N, OR PW PACKAGE  
(TOP VIEW)**



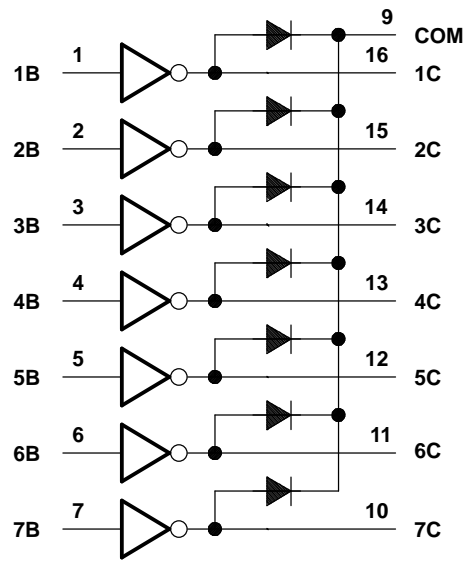
## ORDERING INFORMATION

$T_A$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 105°C	PDIP (N)	Tube of 425	ULN2003AIN	ULN2003AIN
	SOIC (D)	Tube of 40	ULN2003AID	ULN2003AI
		Reel of 2500	ULN2003AIDR	
	TSSOP (PW)	Reel of 2000	ULN2003AIPWR	UN2003AI

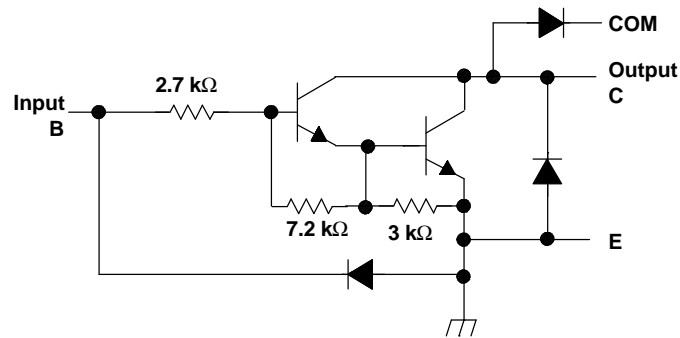


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LOGIC DIAGRAM



SCHEMATICS (EACH DARLINGTON PAIR)



All resistor values shown are nominal.

## Absolute Maximum Ratings<sup>(1)</sup>

at 25°C free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Collector-emitter voltage		50	V
	Clamp diode reverse voltage <sup>(2)</sup>		50	V
$V_I$	Input voltage <sup>(2)</sup>		30	V
	Peak collector current <sup>(3)(4)</sup>		500	mA
$I_{OK}$	Output clamp current		500	mA
	Total emitter-terminal current		-2.5	A
$T_A$	Operating free-air temperature range	-40	105	°C
$\theta_{JA}$	Package thermal impedance <sup>(3)(4)</sup>	D package	73	°C/W
		N package	67	
		PW package	108	
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.
- (3) Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Electrical Characteristics

 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(\text{on})}$	On-state input voltage	5	$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$			2.4	V
				$I_C = 250\text{ mA}$			2.7	
				$I_C = 300\text{ mA}$			3	
$V_{CE(\text{sat})}$	Collector-emitter saturation voltage	4	$I_I = 250\ \mu\text{A}$ , $I_C = 100\text{ mA}$		0.9	1.1	V	
			$I_I = 350\ \mu\text{A}$ , $I_C = 200\text{ mA}$		1	1.3		
			$I_I = 500\ \mu\text{A}$ , $I_C = 350\text{ mA}$		1.2	1.6		
$I_{CEX}$	Collector cutoff current	1	$V_{CE} = 50\text{ V}$ , $I_I = 0$			50	$\mu\text{A}$	
$V_F$	Clamp forward voltage	7	$I_F = 350\text{ mA}$		1.7	2	V	
$I_{I(\text{off})}$	Off-state input current	2	$V_{CE} = 50\text{ V}$ , $I_C = 500\ \mu\text{A}$	50	65		$\mu\text{A}$	
$I_I$	Input current	3	$V_I = 3.85\text{ V}$		0.93	1.35	mA	
$I_R$	Clamp reverse current	6	$V_R = 50\text{ V}$			50	$\mu\text{A}$	
$C_i$	Input capacitance		$V_I = 0$ , $f = 1\text{ MHz}$		15	25	pF	

**ULN2003AI**  
**HIGH-VOLTAGE, HIGH-CURRENT**  
**DARLINGTON TRANSISTOR ARRAY**



SLRS054B–JULY 2003–REVISED FEBRUARY 2005

**Electrical Characteristics**

$T_A = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(\text{on})}$	On-state input voltage	5	$V_{CE} = 2\text{ V}$	$I_C = 200\text{ mA}$			2.7	V
				$I_C = 250\text{ mA}$			2.9	
				$I_C = 300\text{ mA}$			3	
$V_{CE(\text{sat})}$	Collector-emitter saturation voltage	4	$I_I = 250\text{ }\mu\text{A}$ ,	$I_C = 100\text{ mA}$		0.9	1.2	V
			$I_I = 350\text{ }\mu\text{A}$ ,	$I_C = 200\text{ mA}$		1	1.4	
			$I_I = 500\text{ }\mu\text{A}$ ,	$I_C = 350\text{ mA}$		1.2	1.7	
$I_{CEX}$	Collector cutoff current	1	$V_{CE} = 50\text{ V}$ ,	$I_I = 0$			100	$\mu\text{A}$
$V_F$	Clamp forward voltage	7	$I_F = 350\text{ mA}$			1.7	2.2	V
$I_{I(\text{off})}$	Off-state input current	2	$V_{CE} = 50\text{ V}$ ,	$I_C = 500\text{ }\mu\text{A}$	30	65		$\mu\text{A}$
$I_I$	Input current	3	$V_I = 3.85\text{ V}$			0.93	1.35	$\text{mA}$
$I_R$	Clamp reverse current	6	$V_R = 50\text{ V}$				100	$\mu\text{A}$
$C_i$	Input capacitance		$V_I = 0$ ,	$f = 1\text{ MHz}$		15	25	$\text{pF}$

**Switching Characteristics**

$T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 8		0.25	1	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high- to low-level output	See Figure 8		0.25	1	$\mu\text{s}$
$V_{OH}$	High-level output voltage after switching	$V_S = 50\text{ V}$ , $I_O \approx 300\text{ mA}$ , See Figure 9	$V_S - 20$			$\text{mV}$

**Switching Characteristics**

$T_A = -40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low- to high-level output	See Figure 8		1	10	$\mu\text{s}$
$t_{PHL}$	Propagation delay time, high- to low-level output	See Figure 8		1	10	$\mu\text{s}$
$V_{OH}$	High-level output voltage after switching	$V_S = 50\text{ V}$ , $I_O \approx 300\text{ mA}$ , See Figure 9	$V_S - 50$			$\text{mV}$

PARAMETER MEASUREMENT INFORMATION

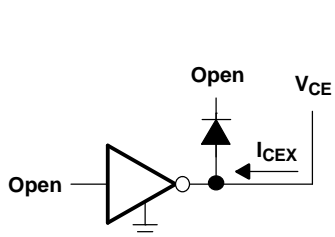


Figure 1.  $I_{CEX}$  Test Circuit

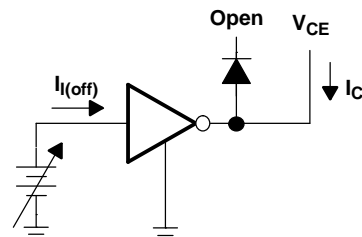


Figure 2.  $I_{I(off)}$  Test Circuit

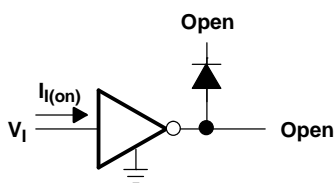
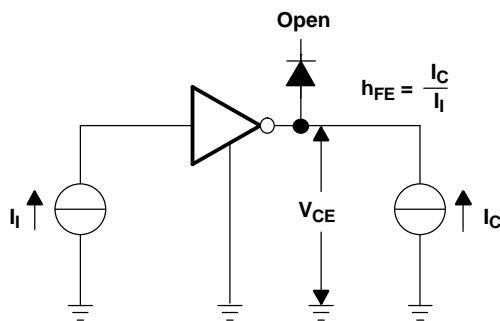


Figure 3.  $I_I$  Test Circuit



NOTE:  $I_I$  is fixed for measuring  $V_{CE(sat)}$ , variable for measuring  $h_{FE}$ .

Figure 4.  $h_{FE}$ ,  $V_{CE(sat)}$  Test Circuit

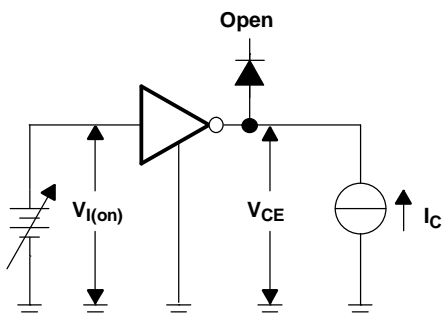


Figure 5.  $V_{I(on)}$  Test Circuit

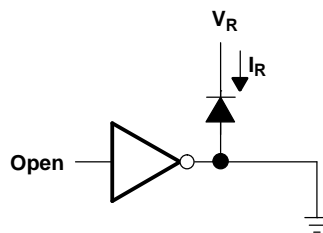


Figure 6.  $I_R$  Test Circuit

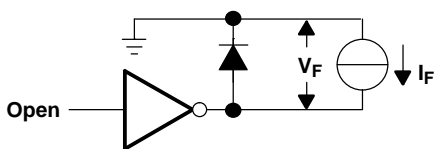


Figure 7.  $V_F$  Test Circuit

PARAMETER MEASUREMENT INFORMATION

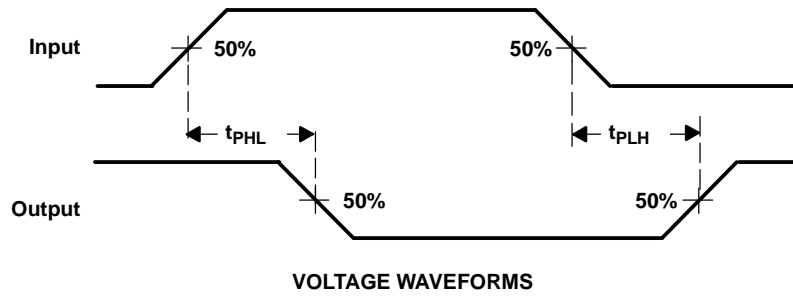
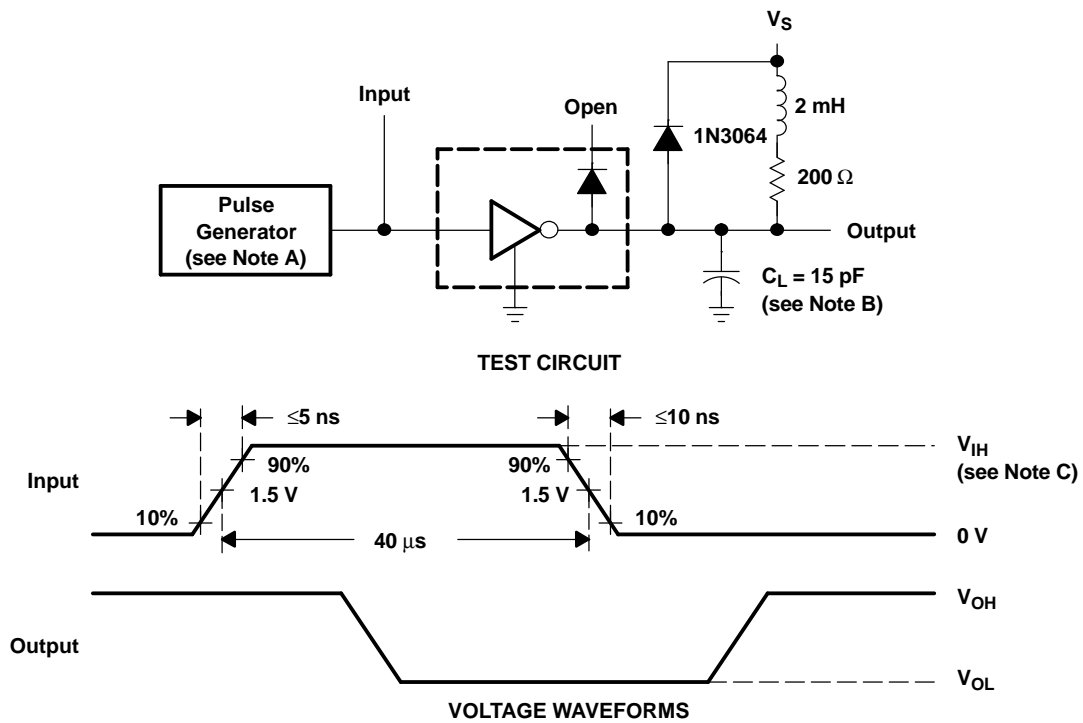


Figure 8. Propagation Delay-Time Waveforms

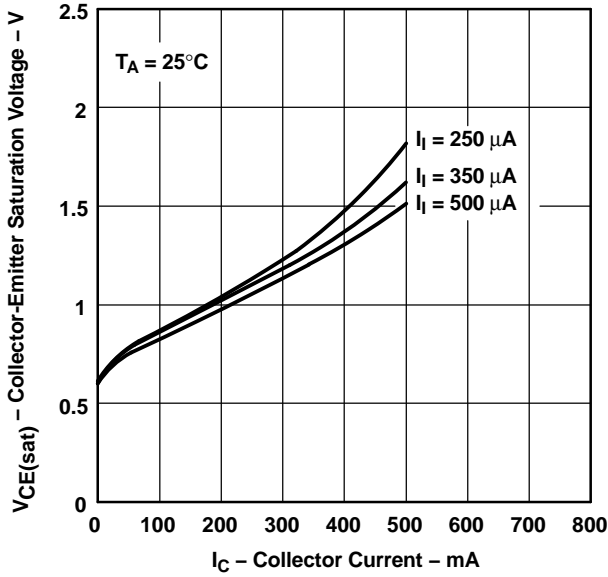


- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.  
 C. For testing,  $V_{IH} = 3 \text{ V}$

Figure 9. Latch-Up Test Circuit and Voltage Waveforms

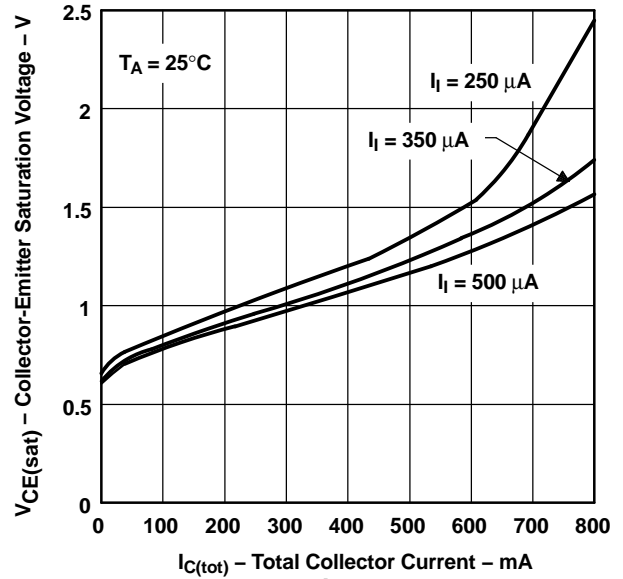
**TYPICAL CHARACTERISTICS**

**COLLECTOR-EMITTER SATURATION VOLTAGE**  
**vs**  
**COLLECTOR CURRENT (ONE DARLINGTON)**



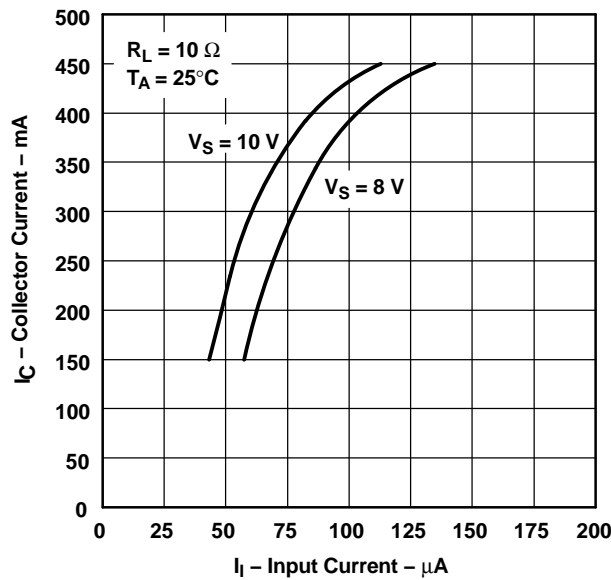
**Figure 10**

**COLLECTOR-EMITTER SATURATION VOLTAGE**  
**vs**  
**TOTAL COLLECTOR CURRENT (TWO DARLINGTONS IN PARALLEL)**



**Figure 11**

**COLLECTOR CURRENT**  
**vs**  
**INPUT CURRENT**



**Figure 12**

THERMAL INFORMATION

D PACKAGE  
 MAXIMUM COLLECTOR CURRENT  
 VS  
 DUTY CYCLE

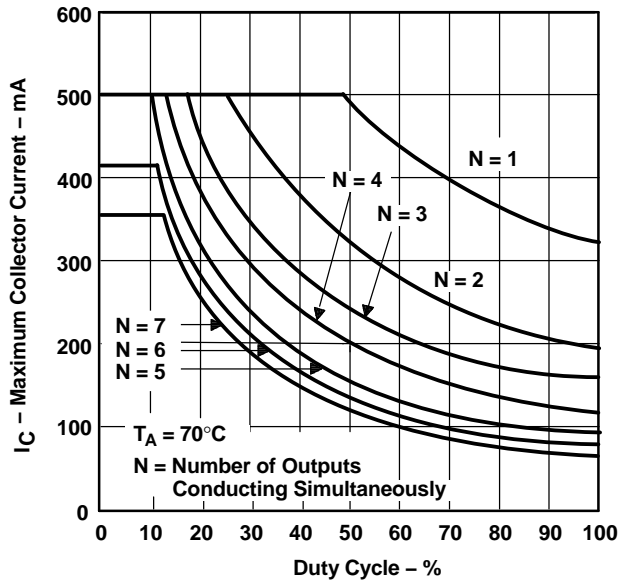


Figure 13

N PACKAGE  
 MAXIMUM COLLECTOR CURRENT  
 VS  
 DUTY CYCLE

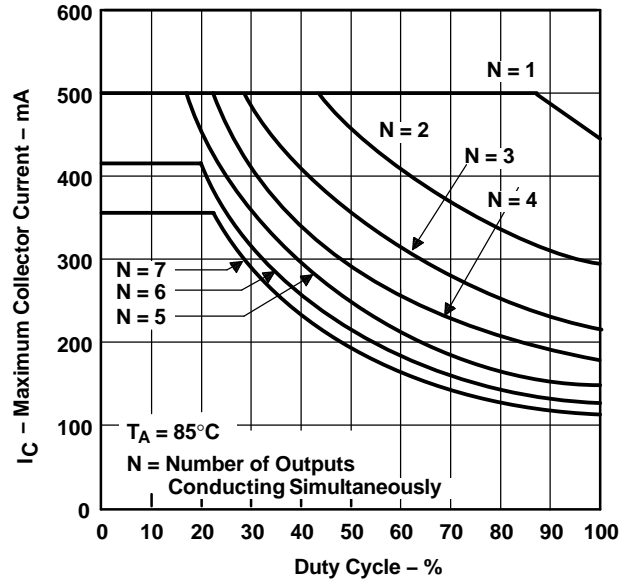
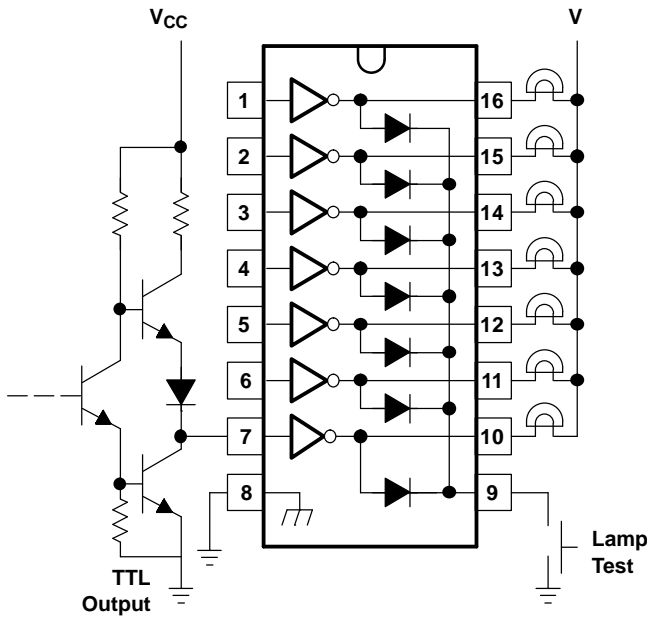


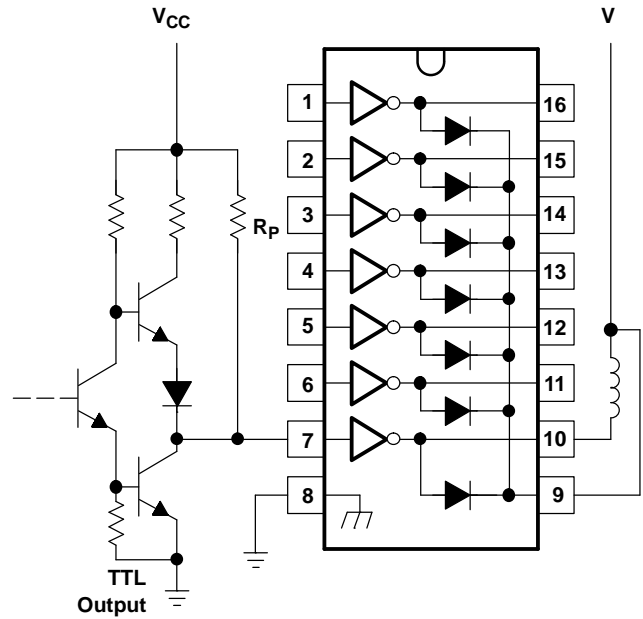
Figure 14



**APPLICATION INFORMATION**



**Figure 15. TTL to Load**



**Figure 16. Use of Pullup Resistors to Increase Drive Current**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ULN2003AID	ACTIVE	SOIC	D	16	40	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
ULN2003AIDR	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
ULN2003AIN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
ULN2003AIPW	ACTIVE	TSSOP	PW	16	90	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
ULN2003AIPWR	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

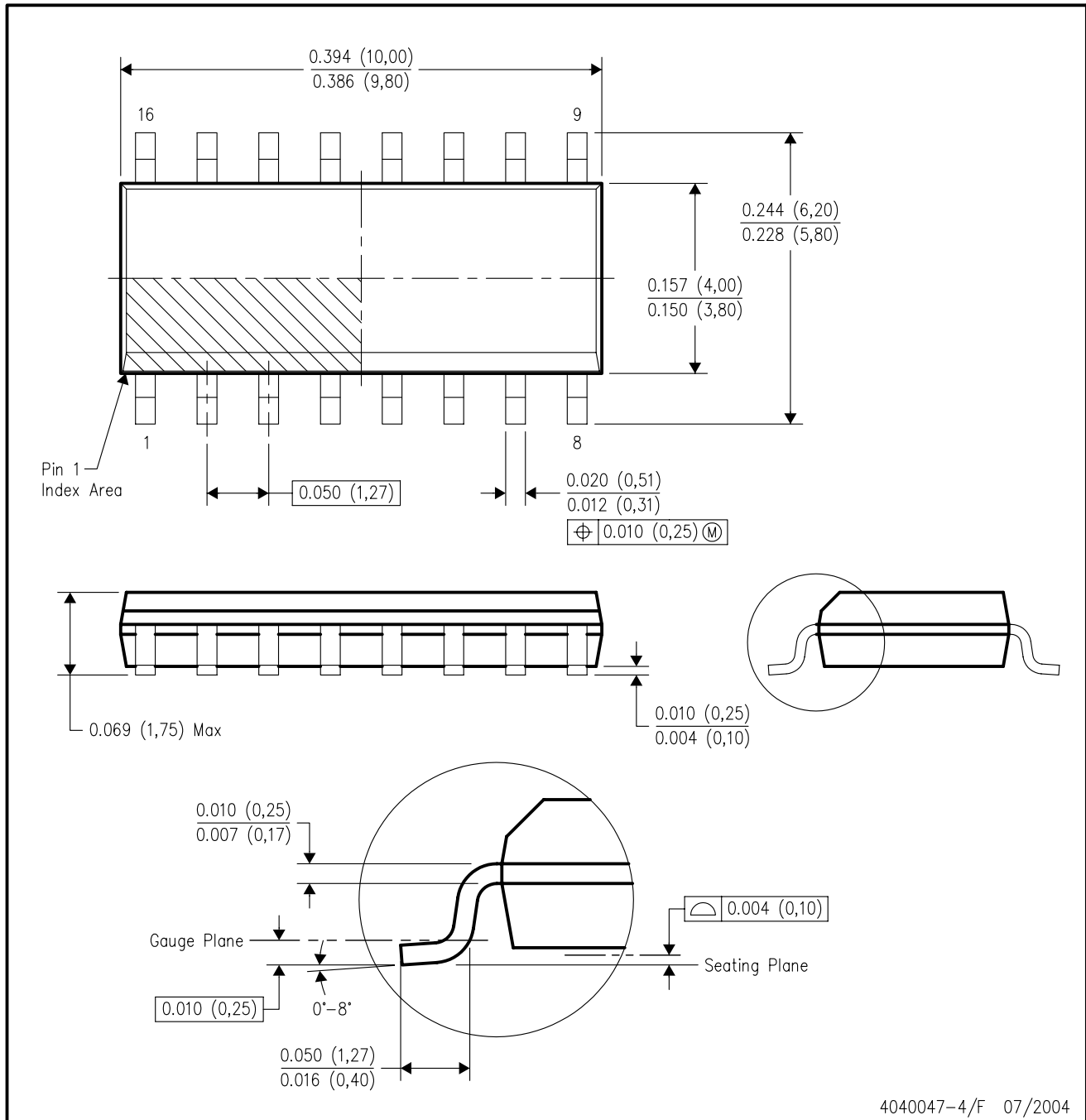
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
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