TPIC2302
3-CHANNEL COMMON-SOURCE POWER DMOS ARRAY

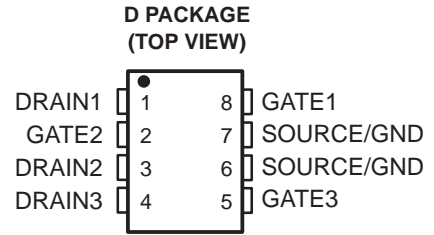- **Low $r_{DS(on)}$ . . . 0.4 Ω Typ**
- **High-Voltage Outputs . . . 60 V**
- **Pulsed Current . . . 5 A Per Channel**
- **Fast Commutation Speed**

D PACKAGE
(TOP VIEW)

```
DRAIN1 [ 1      8 ] GATE1
GATE2  [ 2      7 ] SOURCE/GND
DRAIN2 [ 3      6 ] SOURCE/GND
DRAIN3 [ 4      5 ] GATE3
```

description

The TPIC2302 is a monolithic power DMOS array that consists of three electrically isolated N-channel enhancement-mode DMOS transistors configured with a common source and open drains. The TPIC2302 is offered in a standard 8-pin small-outline surface-mount (D) package.

The TPIC2302 is characterized for operation over the case temperature range of −40°C to 125°C.

schematic
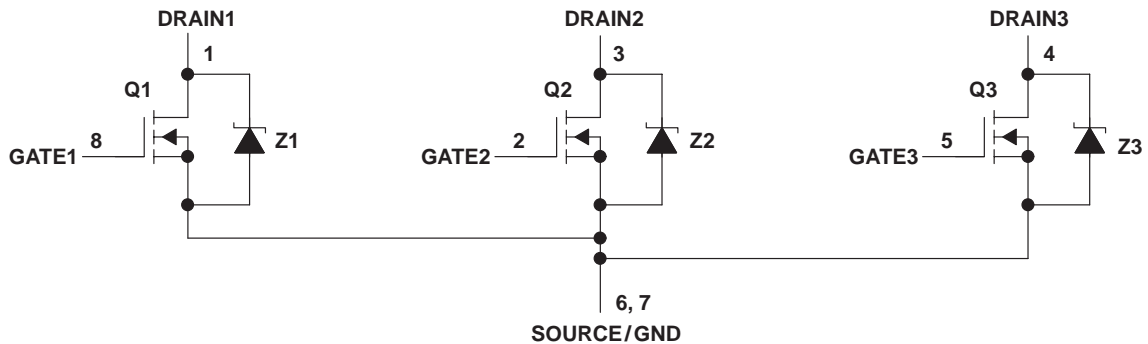
absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Drain-to-source voltage, V_{DS}	60 V
Gate-to-source voltage, V_{GS}	±20 V
Continuous drain current, each output, all outputs on, T_C = 25°C	1 A
Pulsed drain current, each output, T_C = 25°C (see Note 1 and Figure 6)	5 A
Single-pulse avalanche energy, T_C = 25°C, E_{AS} (see Figures 4 and 16)	9 mJ
Continuous total power dissipation at (or below) T_C = 25°C	0.95 W
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating case temperature range, T_C	−40°C to 125°C
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Pulse duration = 10 ms, duty cycle = 2%

TEXAS INSTRUMENTS

electrical characteristics, $T_C = 25°C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-to-source breakdown voltage	$I_D = 250 \ \mu A$,	$V_{GS} = 0$	60			V
$V_{GS(th)}$	Gate-to-source threshold voltage	$I_D = 1 \ mA$,	$V_{DS} = V_{GS}$	1.5	1.85	2.2	V
$V_{DS(on)}$	Drain-to-source on-state voltage	$I_D = 1 \ A$, See Notes 2 and 3	$V_{GS} = 10 \ V$,		0.4	0.475	V
$V_{F(SD)}$	Forward on-state voltage, source-to-drain	$I_S = 1 \ A$, $V_{GS} = 0$ (Z1, Z2, Z3), See Notes 2 and 3			0.9	1.1	V
I_{DSS}	Zero-gate-voltage drain current	$V_{DS} = 48 \ V$, $V_{GS} = 0$	$T_C = 25°C$		0.05	1	μA
			$T_C = 125°C$		0.5	10	
I_{GSSF}	Forward gate current, drain short circuited to source	$V_{GS} = 16 \ V$,	$V_{DS} = 0$		10	100	nA
I_{GSSR}	Reverse gate current, drain short circuited to source	$V_{SG} = 16 \ V$,	$V_{DS} = 0$		10	100	nA
I_{lkg}	Leakage current, drain-to-GND	$V_R = 48 \ V$	$T_C = 25°C$		0.05	1	μA
			$T_C = 125°C$		0.5	10	
$r_{DS(on)}$	Static drain-to-source on-state resistance	$V_{GS} = 10 \ V$, $I_D = 1 \ A$, See Notes 2 and 3 and Figures 6 and 7	$T_C = 25°C$		0.4	0.475	Ω
			$T_C = 125°C$		0.63	0.7	
g_{fs}	Forward transconductance	$V_{DS} = 10 \ V$, See Notes 2 and 3	$I_D = 0.5 \ A$,	0.85	1.02		S
C_{iss}	Short-circuit input capacitance, common source				115	145	pF
C_{oss}	Short-circuit output capacitance, common source	$V_{DS} = 25 \ V$, f = 1 MHz	$V_{GS} = 0$,		60	75	
C_{rss}	Short-circuit reverse-transfer capacitance, common source				30	40	

NOTES: 2. Technique should limit $T_J - T_C$ to 10°C maximum, pulse duration ≤ 5 ms.
3. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

source-to-drain diode characteristics, $T_C = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{rr(SD)}$	Reverse-recovery time	$I_S = 0.5 \ A$, $V_{GS} = 0$, di/dt = 100 A/μs,	$V_{DS} = 48 \ V$, See Figure 1		65		ns
Q_{RR}	Total diode charge				0.03		μC

resistive-load switching characteristics, $T_C = 25°C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Turn-on delay time			21	42	
$t_{d(off)}$	Turn-off delay time	V_{DD} = 25 V, R_L = 50 Ω, t_{r1} = 10 ns,		20	40	ns
t_{r2}	Rise time	t_{f1} = 10 ns, See Figure 2		5	10	
t_{f2}	Fall time			13	26	
Q_g	Total gate charge			3.1	3.8	
$Q_{gs(th)}$	Threshold gate-to-source charge	V_{DS} = 48 V, I_D = 0.5 A, V_{GS} = 10 V, See Figure 3		0.4	0.5	nC
Q_{gd}	Gate-to-drain charge			1.3	1.6	
L_D	Internal drain inductance			5		nH
L_S	Internal source inductance			5		
R_g	Internal gate resistance			0.25		Ω

thermal resistance

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	All outputs with equal power, See Note 4		130		°C/W
$R_{\theta JP}$	Junction-to-pin thermal resistance			44		

NOTE 4: Package mounted on an FR4 printed-circuit board with no heat sink
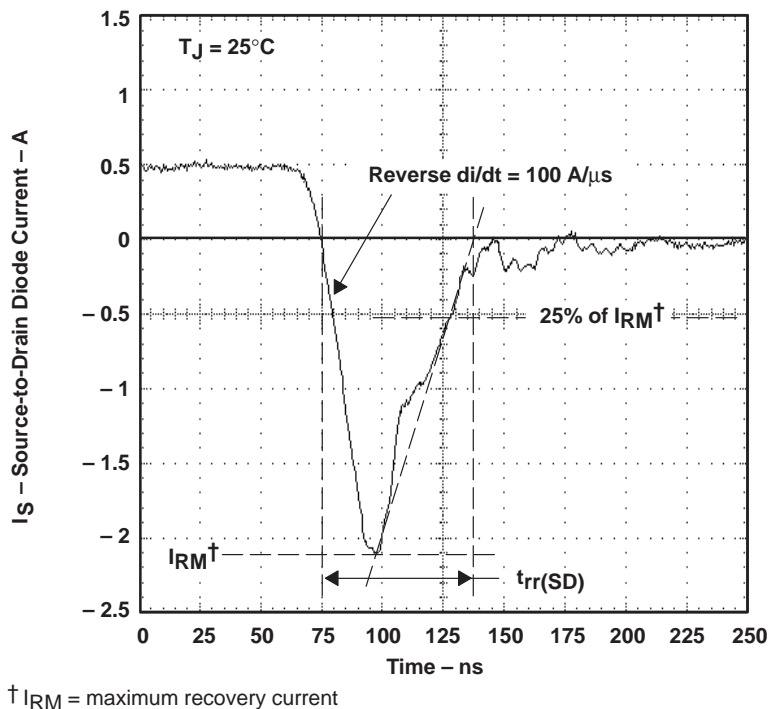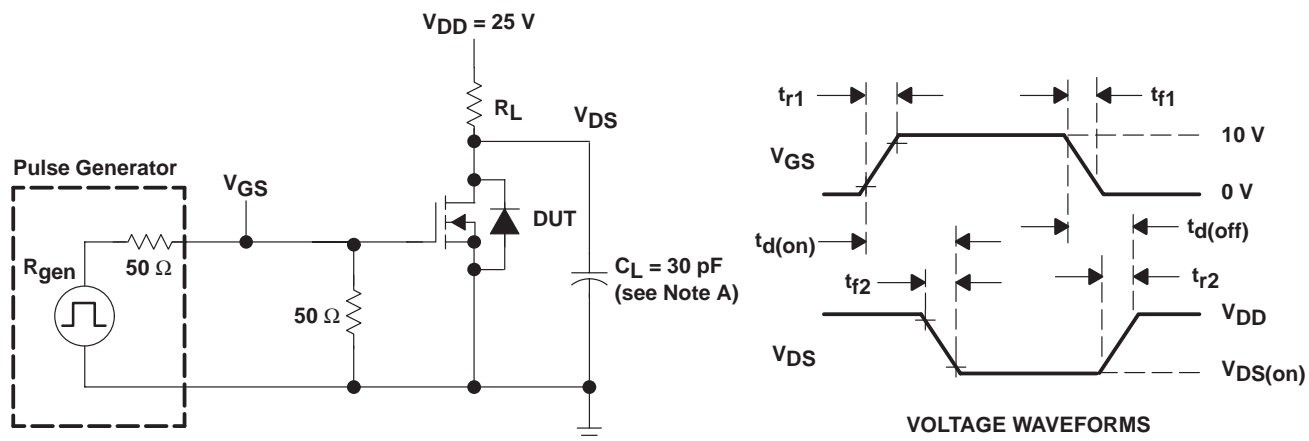
PARAMETER MEASUREMENT INFORMATION

† I_{RM} = maximum recovery current

Figure 1. Reverse-Recovery-Current Waveform of Source-to-Drain Diode

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

NOTE A: C_L includes probe and jig capacitance.

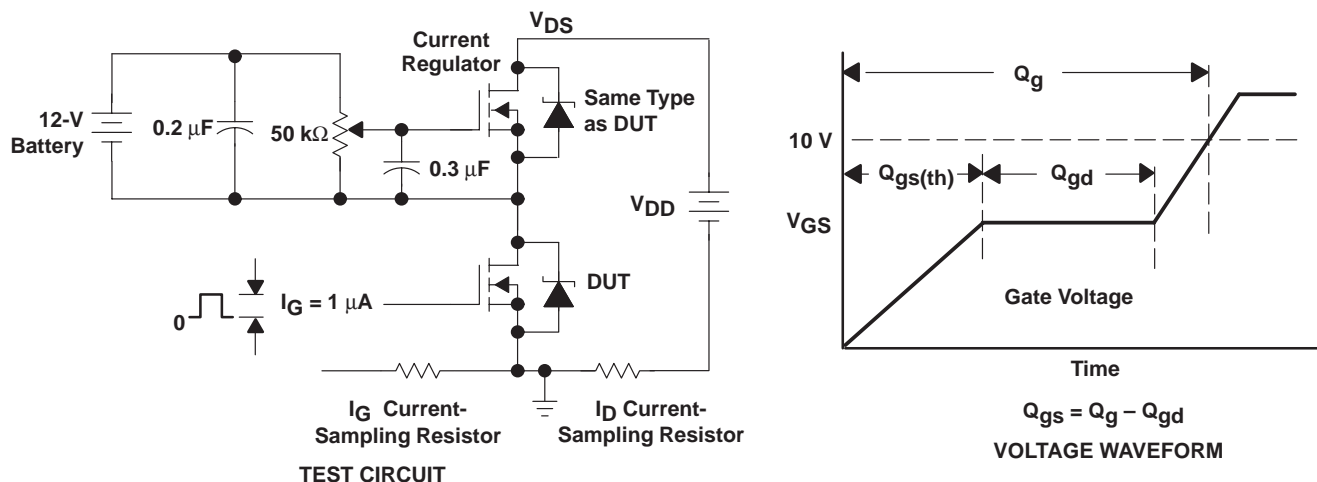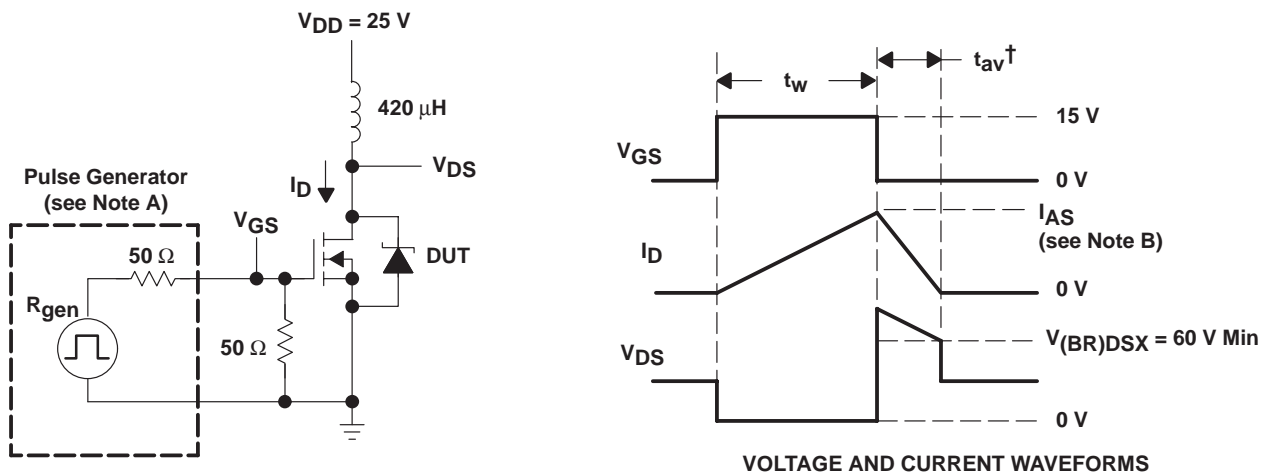**Figure 2. Resistive-Switching Test Circuit and Voltage Waveforms**

$$Q_{gs} = Q_g - Q_{gd}$$

VOLTAGE WAVEFORM

TEST CIRCUIT

Figure 3. Gate-Charge Test Circuit and Voltage Waveform

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

VOLTAGE AND CURRENT WAVEFORMS

† Non-JEDEC symbol for avalanche time

NOTES: A.   The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50\ \Omega$.
         B.   Input pulse duration (t_w) is increased until peak current $I_{AS} = 5$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{AS} \times V_{(BR)DSX} \times t_{av}}{2} = 9$ mJ, where t_{av} = avalanche time.

Figure 4. Single-Pulse Avalanche-Energy Test Circuit and Waveforms
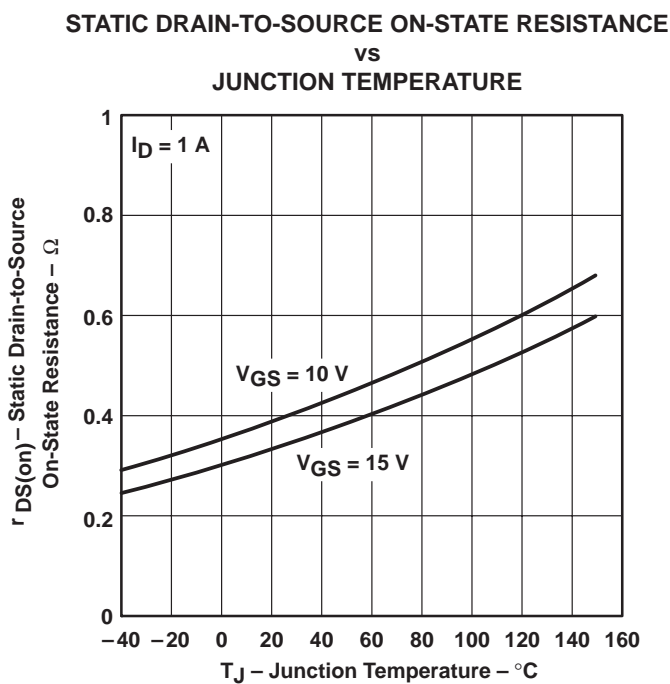
TYPICAL CHARACTERISTICS
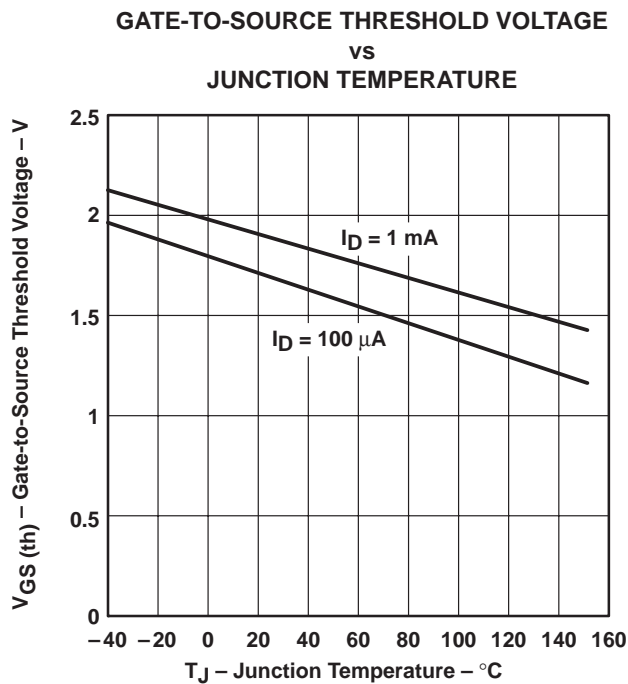
GATE-TO-SOURCE THRESHOLD VOLTAGE
vs
JUNCTION TEMPERATURE

Figure 5

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
vs
JUNCTION TEMPERATURE

Figure 6

TYPICAL CHARACTERISTICS

STATIC DRAIN-TO-SOURCE ON-STATE RESISTANCE
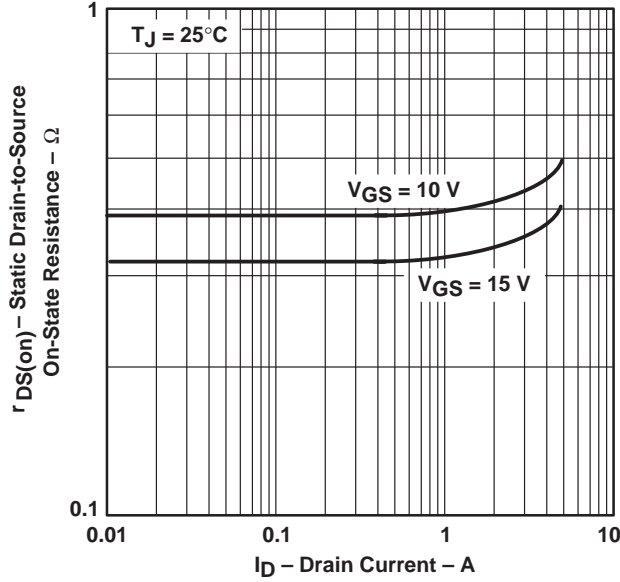vs
DRAIN CURRENT

Figure 7

DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE

Figure 8
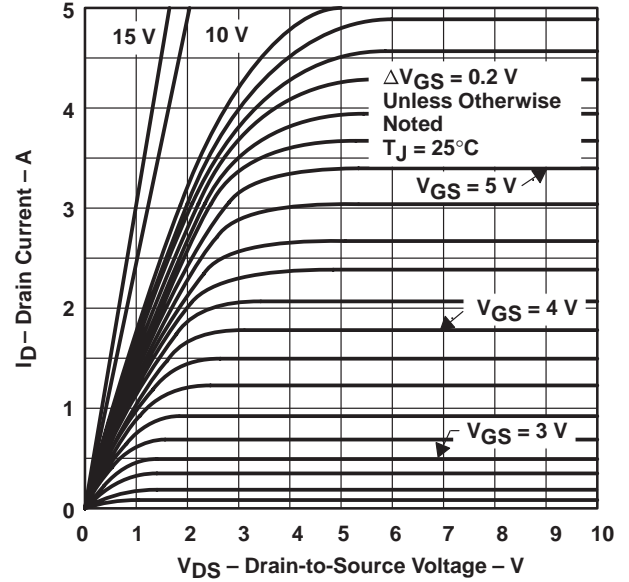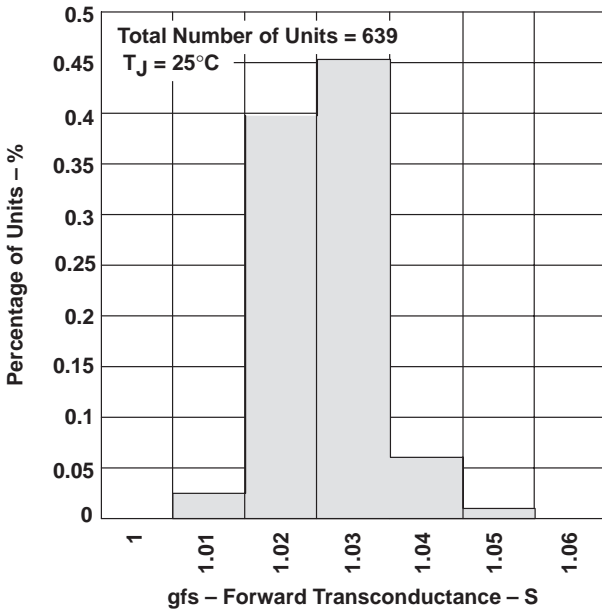
DISTRIBUTION OF
FORWARD TRANSCONDUCTANCE
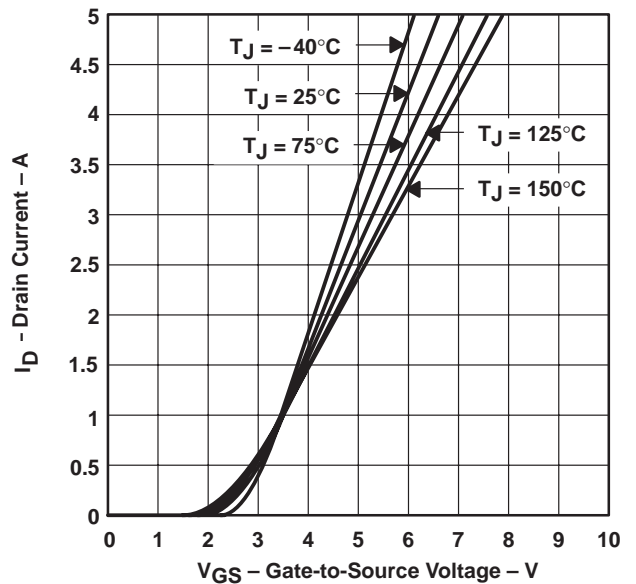

Figure 9

DRAIN CURRENT
vs
GATE-TO-SOURCE VOLTAGE

Figure 10

TEXAS
INSTRUMENTS

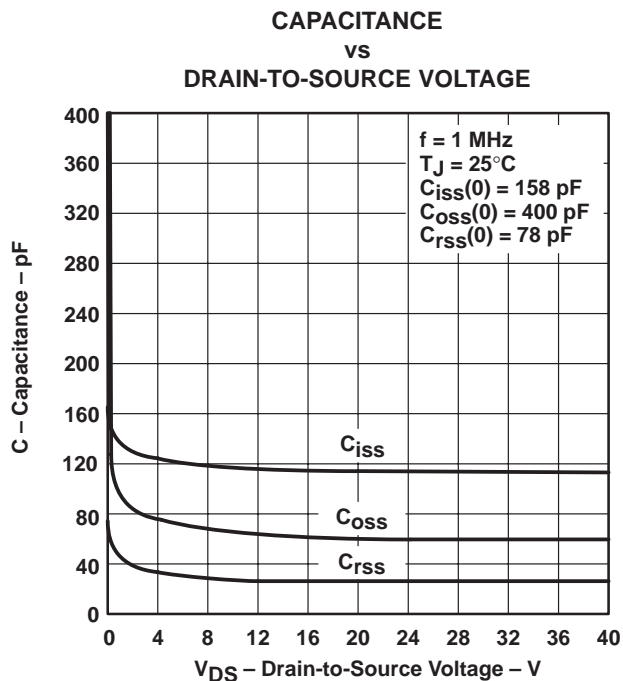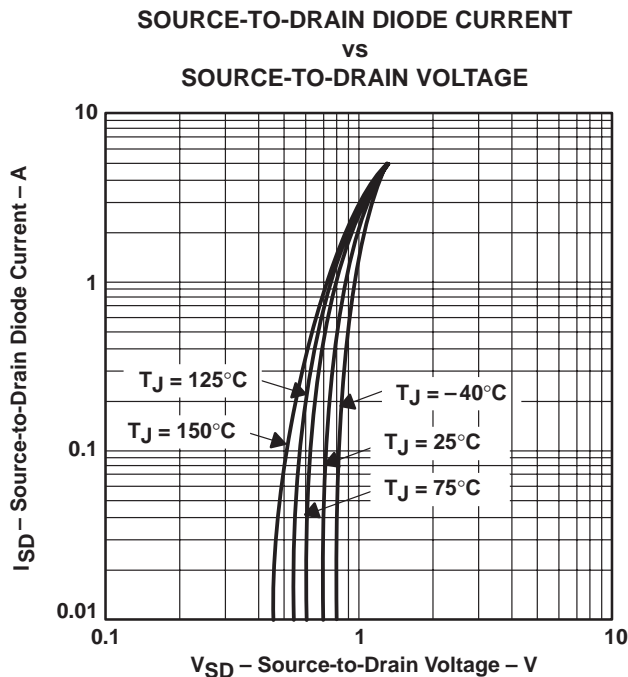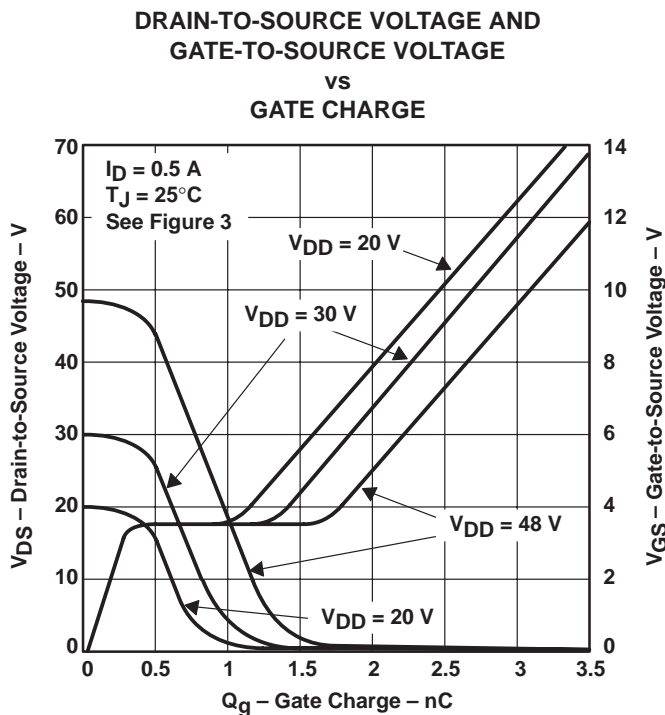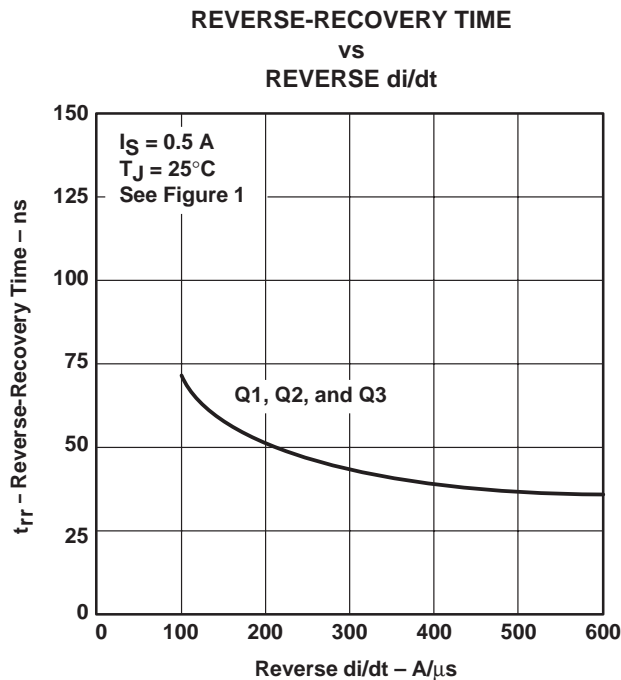POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

TYPICAL CHARACTERISTICS

**CAPACITANCE
vs
DRAIN-TO-SOURCE VOLTAGE**

$f = 1$ MHz
$T_J = 25°C$
$C_{iss}(0) = 158$ pF
$C_{oss}(0) = 400$ pF
$C_{rss}(0) = 78$ pF

Figure 11

**SOURCE-TO-DRAIN DIODE CURRENT
vs
SOURCE-TO-DRAIN VOLTAGE**

$T_J = 125°C$
$T_J = 150°C$
$T_J = -40°C$
$T_J = 25°C$
$T_J = 75°C$

Figure 12

**DRAIN-TO-SOURCE VOLTAGE AND
GATE-TO-SOURCE VOLTAGE
vs
GATE CHARGE**

$I_D = 0.5$ A
$T_J = 25°C$
See Figure 3

$V_{DD} = 20$ V
$V_{DD} = 30$ V
$V_{DD} = 48$ V
$V_{DD} = 20$ V

Figure 13

**REVERSE-RECOVERY TIME
vs
REVERSE di/dt**

$I_S = 0.5$ A
$T_J = 25°C$
See Figure 1

Q1, Q2, and Q3

Figure 14

THERMAL INFORMATION

MAXIMUM DRAIN CURRENT
vs
DRAIN-TO-SOURCE VOLTAGE
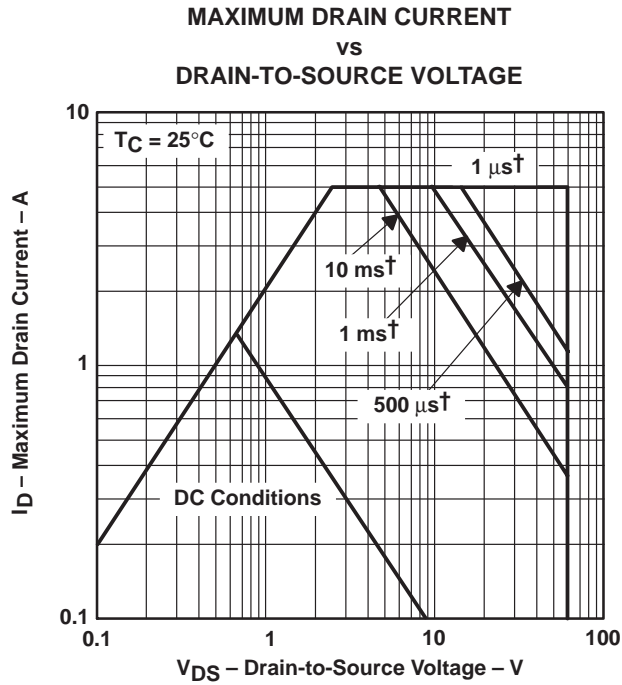
† Less than 0.1 duty cycle

Figure 15

MAXIMUM PEAK-AVALANCHE CURRENT
vs
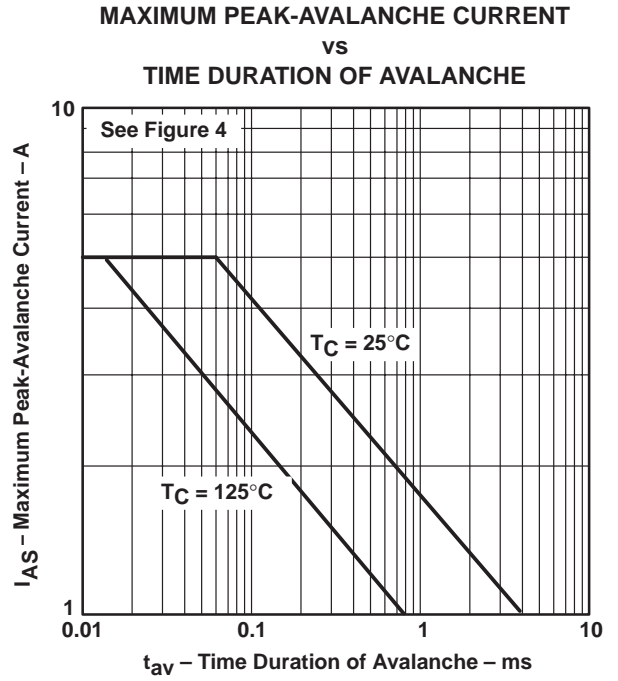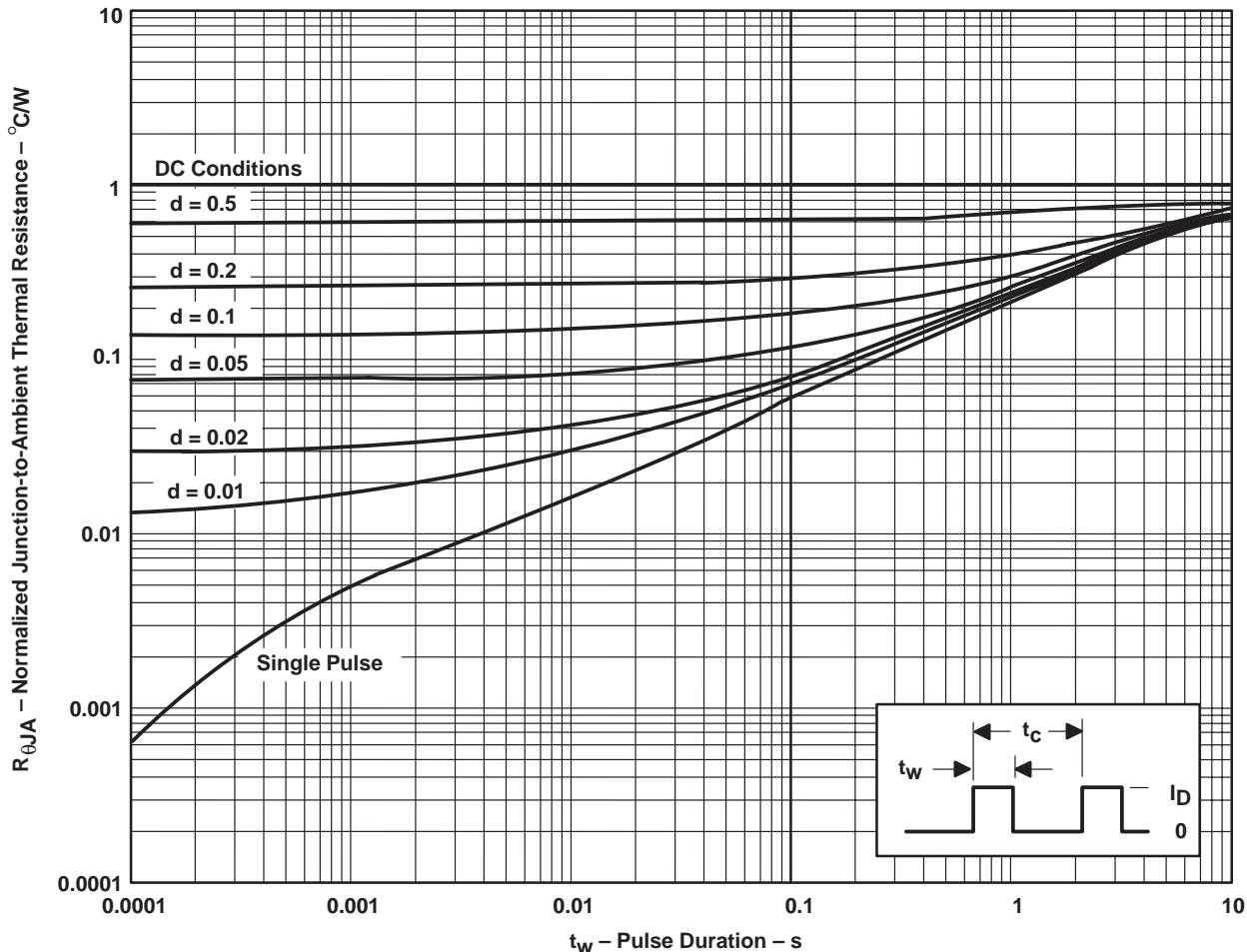**TIME DURATION OF AVALANCHE**

Figure 16

THERMAL INFORMATION

D PACKAGE†
NORMALIZED JUNCTION-TO-AMBIENT THERMAL RESISTANCE
vs
PULSE DURATION

† Device mounted on FR4 printed-circuit board with no heat sink

NOTE A: $Z_{\theta A}(t) = r(t) R_{\theta JA}$
t_W = pulse duration
t_C = cycle time
d = duty cycle = t_W/t_C

Figure 17

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