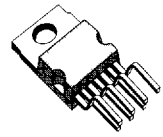
SGS-THOMSON MICROELECTRONICS

TDA8178FS

TV VERTICAL DEFLECTION BOOSTER

- POWER AMPLIFIER
- FLYBACK SUPPLY VOLTAGE SEPARATED
- THERMAL PROTECTION
- REFERENCE VOLTAGE



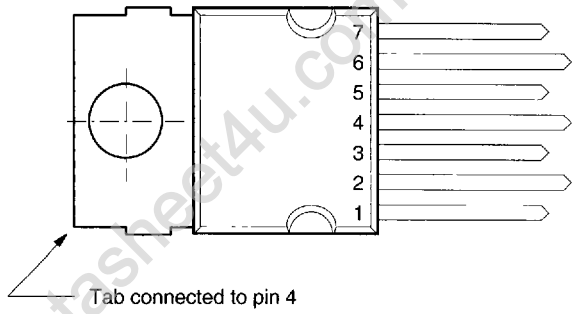
HEPTAWATT
(Plastic Package)

ORDER CODE : TDA8178FS

DESCRIPTION

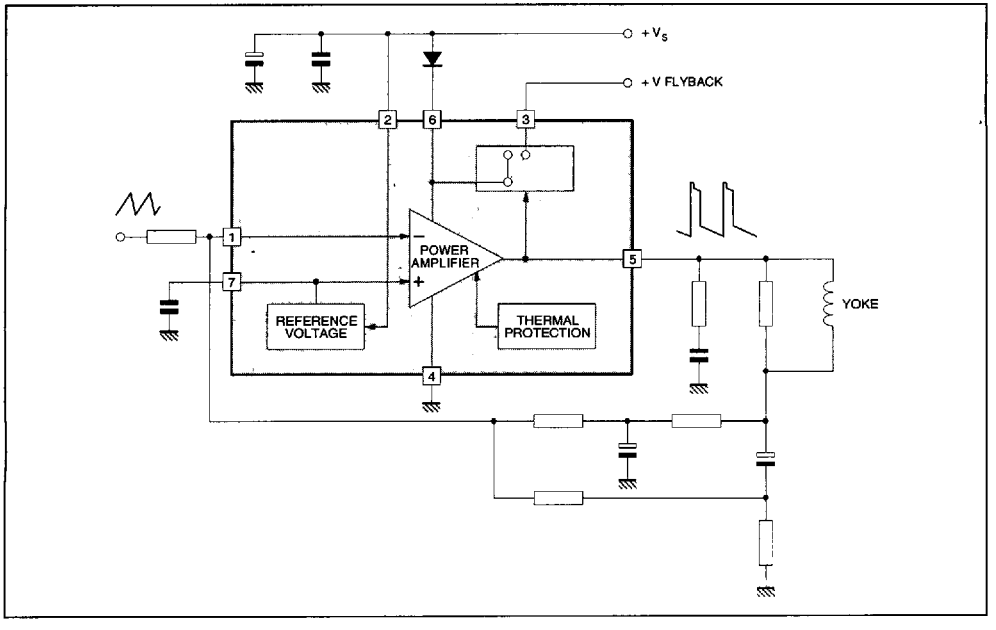
Designed for monitors and high performance TVs, the TDA8178FS vertical deflection booster is able to work with a flyback voltage more than the double of V_S.
The TDA8178FS operates with supplies up to 42V, flyback output up to 92V and provides up to 2App output current to drive to yoke.
The TDA8178FS is offered in HEPTAWATT package.

PIN CONNECTIONS

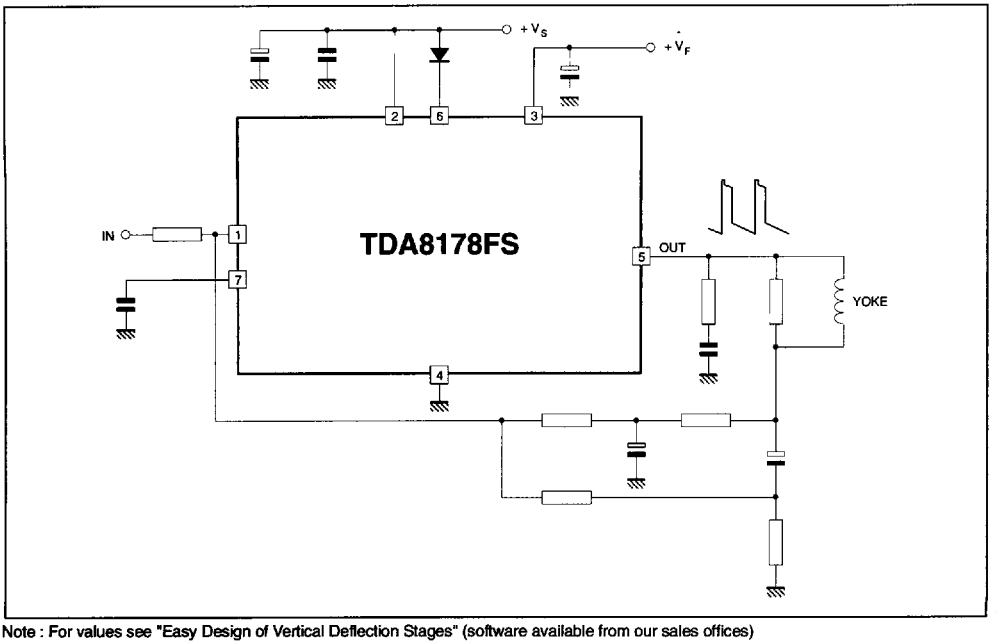


8178F01.EPS

BLOCK DIAGRAM



APPLICATION CIRCUIT



Note : For values see "Easy Design of Vertical Deflection Stages" (software available from our sales offices)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage (pin 2)	50	V
V_F	Flyback Supply Voltage	100	V
$V_F - V_S$	Difference between Flyback Supply Voltage and Supply Voltage	50	V
V_1 , V_7	Amplifier Input Voltage	+ V_S	
I_O	Output Peak Current Non-repetitive, t = 2ms f = 50 or 60Hz, t ≤ 10µs f = 50 or 60Hz, t > 10µs	 2 2 1.8	A
I_3	Pin 3 Peak Flyback Current at f = 50 or 60Hz, $t_{fly} \leq 1.5$ms	1.8	A
P_{tot}	Total Power Dissipation at $T_C = 70°C$	20	W
T_{stg}	Storage Temperature	- 40, + 150	°C
T_j	Junction Temperature	0, +150	°C

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THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Junction-case Thermal Resistance	Max.	3	°C/W

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ELECTRICAL CHARACTERISTICS

(V_S = 42V, $T_A = 25°C$, unless otherwise specified)(refer to the test circuits - see Figure 1 next page)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_S	Operating Supply Voltage Range		10		42	V
I_2	Pin 2 Quiescent Current	$I_3 = 0$ $I_5 = 0$		10	20	mA
I_6	Pin 6 Quiescent Current	$I_3 = 0$ $I_5 = 0$		20	40	mA
I_1	Amplifier Bias Current	V_1 = 1V		- 0.2	- 1	µA
V_5	Quiescent Output Voltage	 V_S = 42V R_a = 3.9kΩ V_S = 35V R_a = 5.6kΩ	 23.4 17	 24.2 17.8	 25 18.5	V
V_{5L}	Output Saturation Voltage to GND	I_5 = 1A		1.2	1.5	V
V_{5H}	Output Saturation Voltage to Supply	$-I_5$ = 1A		2.2	2.6	V
V_{D5-6}	Diode Forward Voltage between Pins 5-6	I_D = 1A		1.5	3	V
V_{D3-6}	Diode Forward Voltage between Pins 3-6	I_D = 1A		1.5	3	V
V_7	Internal Reference		2.1	2.2	2.3	V
$\Delta V_7/\Delta V_S$	Reference Voltage Drift versus V_S	V_S = 24 to 42V		2	4	mV/V
K_T	Reference Voltage Drift versus T_j	T_j = 0 to 125°C $K_T = \frac{\Delta V_7}{\Delta T_j} \frac{10^6}{V_7}$		100	150	ppm/°C
R_1	Input Resistance			200		kΩ
T_j	Junction Temperature for Thermal Shutdown			140		°C

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FIGURE 1 : DC Test Circuits

Figure 1a : Measurement of I_1,I_2,I_6,V_7, $\Delta V_7/\Delta V_S$

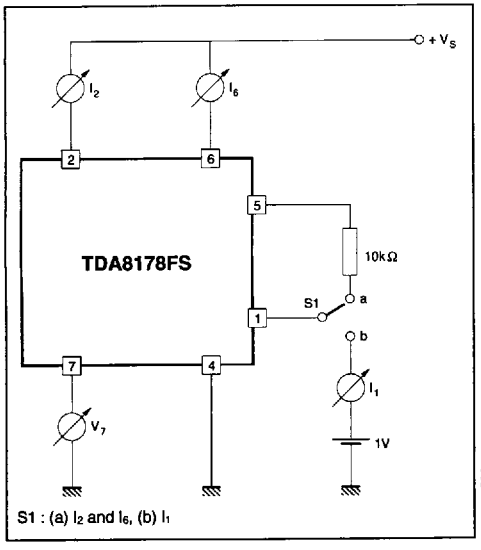

Figure 1b : Measurement of V_{5H}

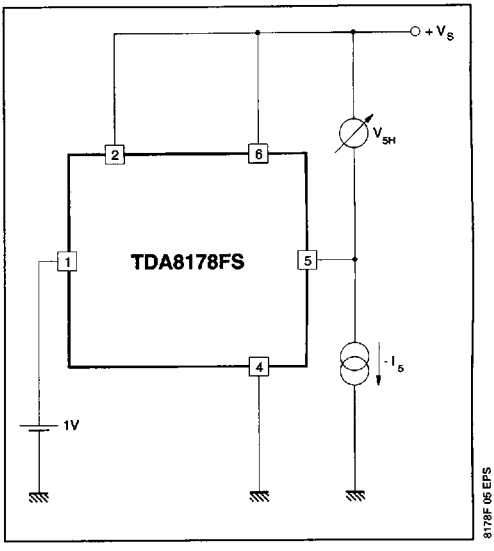

Figure 1c : Measurement of V_{5L}

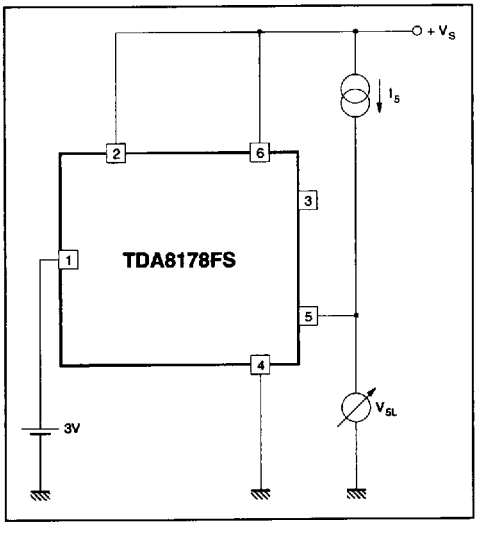

Figure 1d : Measurement of V_5

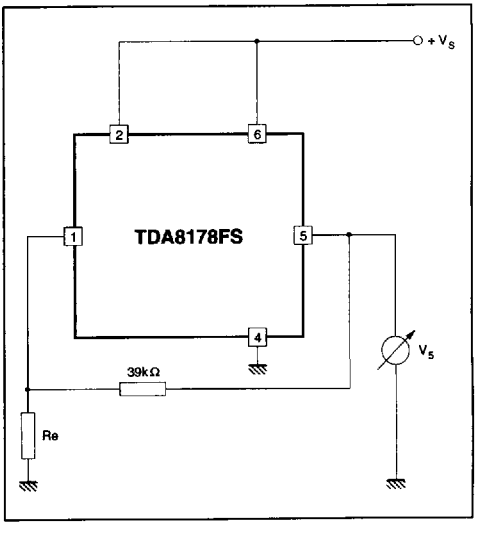

Figure 2 : SOA of Each Output Power Transistor at $T_A = 25^{\circ}C$