Preliminary Data Sheet, DS3, July 2003

SLICOFI-2/-2S

Dual Channel Subscriber Line Interface Codec Filter

PEB 3265, Version 1.5

PEB 3264, Version 1.4

Wired Communications

Infineon technologies

Never stop thinking.

ABM®, ACE®, AOP®, ARCOFI®, ASM®, ASP®, DigiTape®, DuSLIC®, EPIC®, ELIC®, FALC®, GEMINAX®, IDEC®, INCA®, IOM®, IPAT®-2, ISAC®, ITAC®, IWE®, IWORX®, MUSAC®, MuSLIC®, OCTAT®, OptiPort®, POTSWIRE®, QUAT®, QuadFALC®, SCOUT®, SICAT®, SICOFI®, SIDEC®, SLICOFI®, SMINT®, SOCRATES®, VINETIC®, 10BaseV®, 10BaseVX® are registered trademarks of Infineon Technologies AG. 10BaseS™, EasyPort™, VDSLite™ are trademarks of Infineon Technologies AG. Microsoft® is a registered trademark of Microsoft Corporation. Linux® is a registered trademark of Linus Torvalds.

The information in this document is subject to change without notice.

Edition 2003-07-14

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany

Attention please!

The information herein is given to describe certain components and shall not be considered as warranted characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Infineon Technologies is an approved CECC manufacturer.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office in Germany or our Infineon Technologies Representatives worldwide (**www.infineon.com**).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Preliminary Data Sheet

Revision History: **2003-07-14** DS3

Previous Version:	Data Sheet DS2
Page	**Subjects (major changes since last revision)**
Page 10	New package option P-TQFP-64-1 added.
Page 11	**“Features SLICOFI-2S PEB 3264” on Page 11**: ITDF and modem performance added.
Page 22	**Table 2 "Performance Characteristics of the DTMF Decoder Algorithm" on Page 22**: Pulse noise influence description updated.
Page 28	**“SLICOFI-2 and SLIC-E/-E2 Interface” on Page 28**: Information updated for SLIC-E/-E2 Version 1.2.
Page 29	**“SLICOFI-2 and SLIC-P Interface” on Page 29**: Information updated for SLIC-P Version 1.2.
Page 31	**“Signal Path and Test Loops” on Page 31**: description updated but figures unchanged.
Page 35	**“Operating Range” on Page 35**: pins IO3j and IO4j added at parameter "analog input pins referred to the ground pin (GNDj)"
Page 52	**“Double-Clocking Mode” on Page 52**: Period PCLK (t_{PCLK}) for double clocking: formula for typ. value modified.
Page 58	New package option P-TQFP-64-1 added.

Table of Contents **Page**

Table of Contents **Page**

List of Figures **Page**

List of Tables

Preface

This Preliminary Data Sheet describes the SLICOFI-2 (PEB 4365) and SLICOFI-2S (PEB 4364) codec devices, which are part of the Dual Channel Subscriber Line Interface Codec Filter (DuSLIC) chip set family.

Synonyms

To simplify matters, the following synonyms are used:

SLICOFI-2x Synonym used for all codec versions SLICOFI-2 and SLICOFI-2S.

SLIC: Synonym used for all SLIC versions SLIC-S/-S2, TSLIC-S, SLIC-E/-E2, TSLIC-E and SLIC-P.

Attention: The TSLIC-S (PEB 4364) and TSLIC-E (PEB 4365) chips are dual channel versions of the SLIC-S (PEB 4264) and SLIC-E (PEB 4265) with identical technical specifications for each channel. Therefore whenever SLIC-S or SLIC-E are mentioned in the specification, also TSLIC-S and TSLIC-E can be deployed.

Organization of this Document

This Preliminary Data Sheet is divided into nine chapters. It is organized as follows:

- **Chapter 1**, **Overview**
  A general description of the device and a list of its key features.
- **Chapter 2**, **Pin Descriptions**
  Detailed description and pin diagram
- **Chapter 3**, **Functional Description**
  The main functions of the device are presented with a functional block diagram.
- **Chapter 4**, **Operating Modes for the DuSLIC Chip Set**
  A brief description of the operating modes.
- **Chapter 5**, **Signal Path and Test Loops**
  Figures of the AC and DC signal path and integrated test loops.
- **Chapter 6**, **Electrical Characteristics**
  Parameters, symbols and limit values.
- **Chapter 7**, **Package Outlines**
  Illustrations and dimensions of the package outlines.
- **Chapter 8**, **Terminology**
  List of abbreviations and description of symbols.
- **Chapter 9**, **Index**

1 Overview

The Subscriber Line Interface Circuit *SLICOFI-2x* is a highly flexible two channel codec solution for analog line circuits. The *SLICOFI-2x* is programmable via software and can be adapted to meet all different standards worldwide.

DuSLIC Architecture

The SLICOFI-2 (PEB 3265) and SLICOFI-2S (PEB 3264) chips are part of the DuSLIC chip set and are designed for use with the SLIC-E/-E2/-P (PEB 4265/-2, PEB 4266) and SLIC-S/-S2 (PEB 4264/-2) devices.

Unlike traditional designs, DuSLIC splits the SLIC function into high-voltage SLIC funtions and low-voltage SLIC functions. The low-voltage functions are handled in the *SLICOFI-2x* device, the high-voltage functions are handled in the SLIC devices.

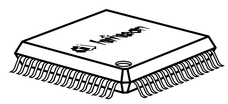
All *SLICOFI-2x codec devices are manufactured using an advanced 0.35 µm 3.3 V CMOS process.*

For further information see **Chapter 3.1**.

Dual Channel Subscriber Line Interface Codec Filter **PEB 3265**
SLICOFI-2x **PEB 3264**

Version 1.5 **CMOS**

1.1 Features SLICOFI-2 PEB 3265[1]



P-MQFP-64-1,-2

P-TQFP-64-1

- Fully programmable dual-channel codec
- Programmable battery feeding with capability for driving long loops
- Internal balanced/unbalanced ringing capability (up to 85 Vrms balanced / 50 Vrms unbalanced)
- External ringing support
- Ground/loop start signaling
- Polarity reversal
- On-hook transmission
- Programmable Teletax (TTX) generation
- Integrated DTMF generator
- Integrated DTMF decoder
- Integrated Caller ID (FSK) generator
- Integrated fax/modem detection–
  Universal Tone Detection (UTD)
- Integrated Line Echo Cancellation unit (LEC)
- Optimized filter structure for modem transmission
- Message waiting lamp support (for PBX applications)
- Three-party conferencing (in PCM/µC mode)
- 8 and 16 kHz PCM Transmission
- IOM-2 or PCM/µC Interface selectable
- Power optimized architecture
- Power management capability (battery switching)
- Integrated test and diagnosis functions (ITDF)
- Specification in accordance with
  ITU-T Recommendation Q.552 for interface Z, ITU-T Recommendation G.712 and applicable LSSGR

1) Features are indicated for the DuSLIC chip set and are partially realized by the SLICOFI-2 codec.

Type	**Package**
PEB 3265, PEB 3264	P-MQFP-64-1 or P-TQFP-64-1

1.2 Features SLICOFI-2S PEB 3264[1)]

- Fully programmable dual-channel codec
- Programmable battery feed with capability for driving long loops
- Internal balanced ringing capability up to 45 Vrms
- External ringing support
- Ground/loop start signaling
- Polarity reversal
- On-hook transmission
- Programmable Teletax (TTX) generation (not available with SLICOFI-2S2)
- Optimized filter structure for modem transmission
- Integrated DTMF generator
- 8 and 16 kHz PCM Transmission
- IOM-2 or PCM/µC Interface selectable
- Power optimized architecture
- Power management capability (battery switching)
- Integrated test and diagnosis functions (ITDF)
- Specification in accordance with
  ITU-T Recommendation Q.552 for interface Z, ITU-T Recommendation G.712 and applicable LSSGR

1) Features are indicated for the DuSLIC chip set and are partially realized by the SLICOFI-2S codec.

1.3 Logic Symbol

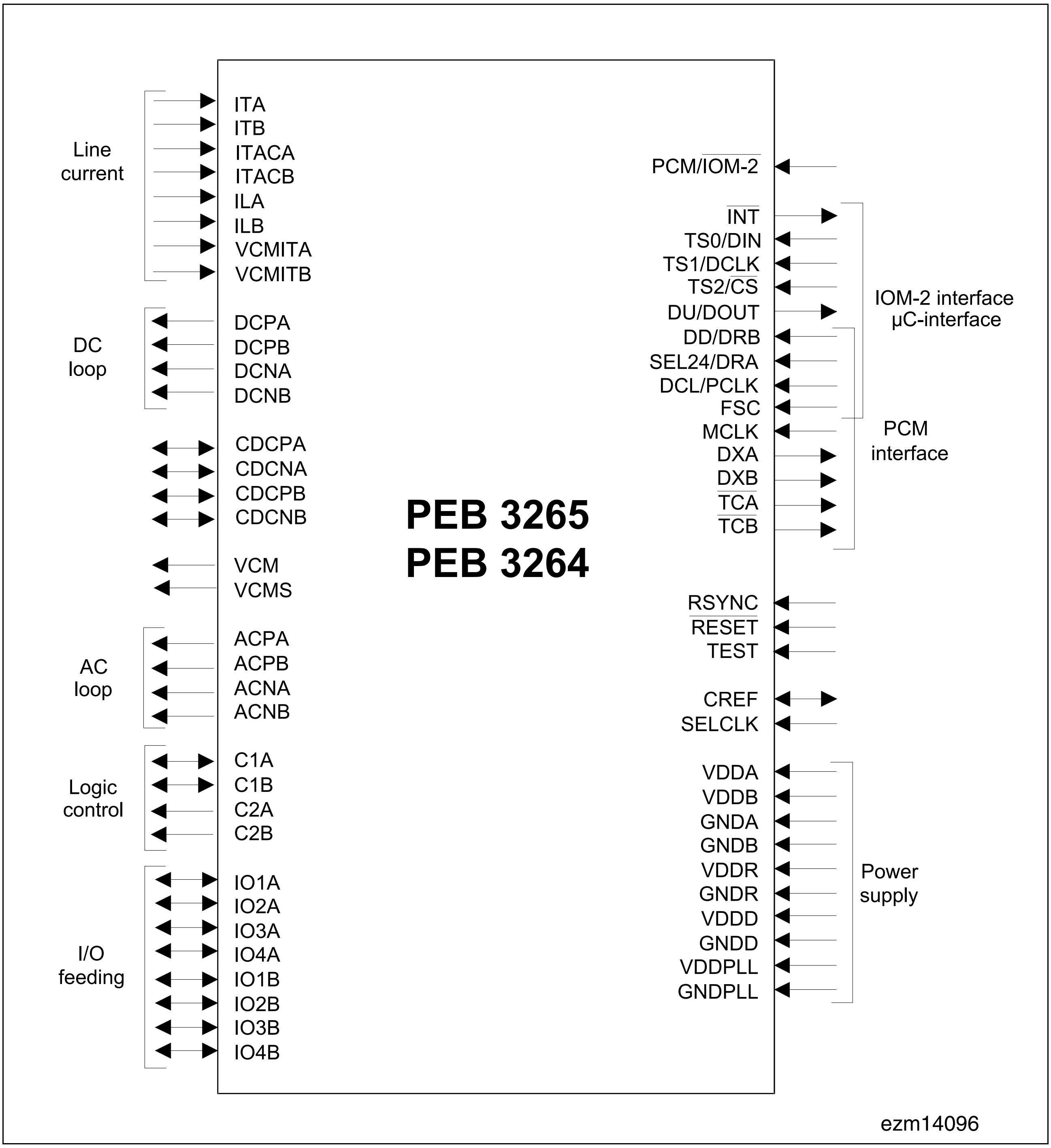


Figure 1 Logic Symbol: *SLICOFI-2x*

2 Pin Descriptions

2.1 Pin Diagram

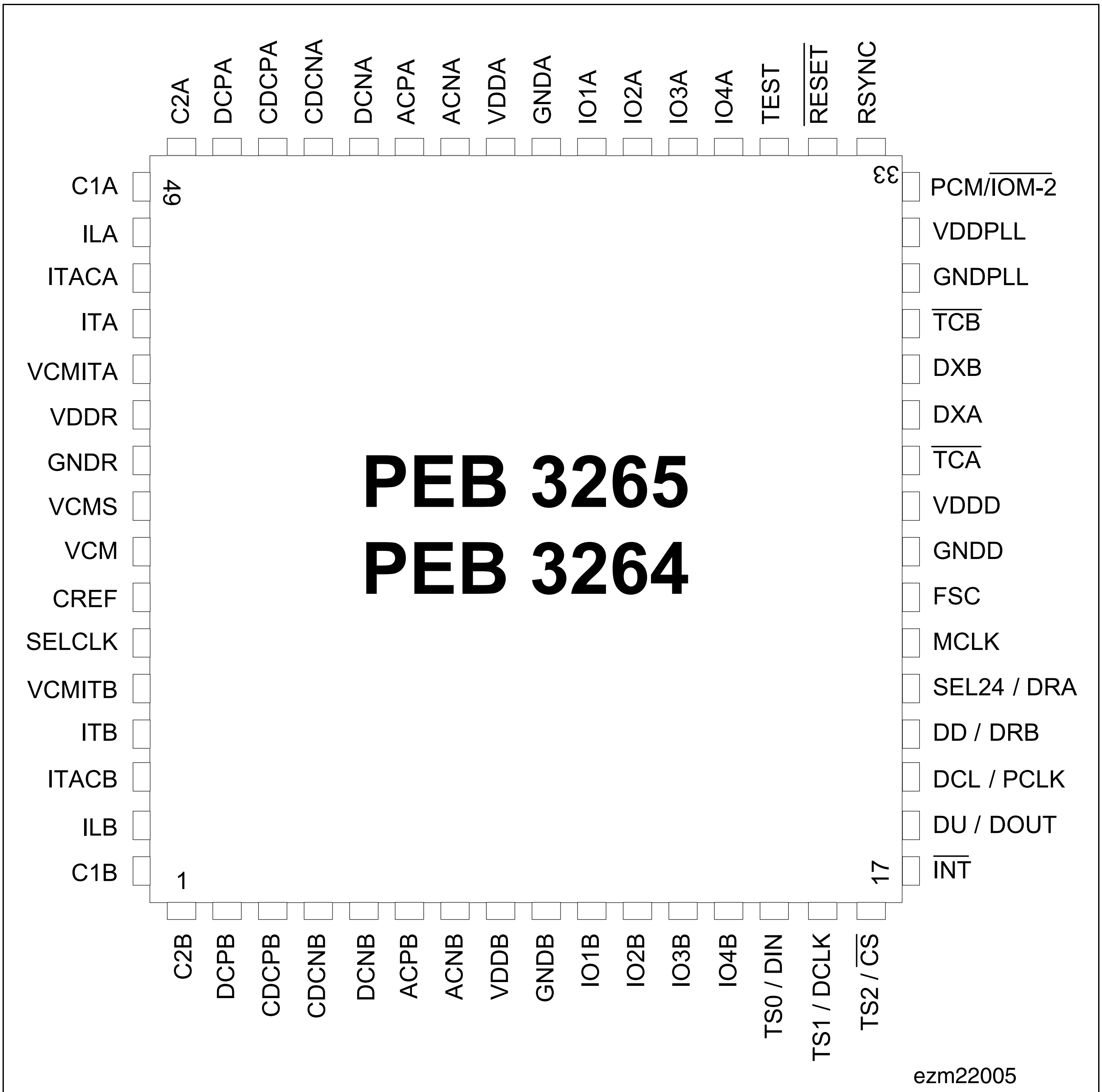


Figure 2 **Pin Configuration:** ***SLICOFI-2x*** (top view)

Table 1 Pin Definitions and Functions *SLICOFI-2x*

Pin No.	Sym-bol	Input (I) Output (O)	Function
1	C2B	O	Ternary logic output for controlling the SLIC operation mode (Channel B)
2	DCPB	O	Two-wire output voltage (DCP) (Channel B)
3	CDCPB	I/O	External capacitance for filtering (Channel B)
4	CDCNB	I/O	External capacitance for filtering (Channel B)
5	DCNB	O	Two-wire output voltage (DCN) (Channel B)
6	ACPB	O	Differential two-wire AC output voltage controlling the RING pin (Channel B)
7	ACNB	O	Differential two-wire AC output voltage controlling the TIP pin (Channel B)
8	VDDB	Power	+3.3 V analog supply voltage (Channel B)
9	GNDB	Power	Analog ground (Channel B)
10	IO1B	I/O	User-programmable I/O pin (Channel B) with relay-driving capability. In external ringing mode, IO1 is used to automatically control and drive the ring relay.
11	IO2B	I/O	User-programmable I/O pin (Channel B) with relay-driving capability. SLICOFI-2 and SLIC-P: connected to pin C3 of SLIC-P, when two supply voltages for voice transmission and internal ringing are used.[1)]
12	IO3B	I/O	User-programmable I/O pin (Channel B) with analog input functionality
13	IO4B	I/O	User-programmable I/O pin (Channel B) with analog input functionality
14	TS0 DIN	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): Time slot selection pin 0 PCM/$\overline{\text{IOM-2}}$ = 1 (µC Interface): Data in
15	TS1 DCLK	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): Time slot selection pin 1 PCM/$\overline{\text{IOM-2}}$ = 1 (µC Interface): Data clock
16	TS2 $\overline{\text{CS}}$	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): Time slot selection Pin 2 PCM/$\overline{\text{IOM-2}}$ = 1 (µC Interface): Chip select, active low

Table 1 Pin Definitions and Functions *SLICOFI-2x* (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
17	$\overline{\text{INT}}$	O	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): not connected PCM/$\overline{\text{IOM-2}}$ = 1 (µC Interface): Interrupt pin, active low[2)]
18	DU DOUT	O O	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): Data upstream, open drain PCM/$\overline{\text{IOM-2}}$ = 1 (µC Interface): Data out, push/pull
19	DCL PCLK	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): Data clock PCM/$\overline{\text{IOM-2}}$ = 1 (PCM Interface): 128 kHz to 8192 kHz PCM clock
20	DD DRB	I I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): Data downstream PCM/$\overline{\text{IOM-2}}$ = 1 (PCM Interface): Receive data input for PCM Highway B
21	SEL24 DRA	I I	PCM/$\overline{\text{IOM-2}}$ =0 (IOM-2 Interface): SEL24 = 0: DCL = 2048 kHz selected SEL24 = 1: DCL = 4096 kHz selected PCM/$\overline{\text{IOM-2}}$ =1 (PCM Interface): Receive Data input for PCM Highway A
22	MCLK	I	PCM/$\overline{\text{IOM-2}}$ = 0 (IOM-2 Interface): not connected PCM/$\overline{\text{IOM-2}}$ = 1 (PCM Interface): master clock when PCM/µC Interface is used, clock rates are 512 kHz, 1536 kHz, 2048 kHz, 4096 kHz, 7168 kHz, 8192 kHz
23	FSC	I	Frame synchronization clock for PCM/µC or IOM-2 interface, 8 kHz, identifies the beginning of the frame, individual time slots are referenced to this input signal.
24	GNDD	Power	Digital ground
25	VDDD	Power	+3.3 V digital supply voltage
26	$\overline{\text{TCA}}$	O	Transmit control output for PCM Highway A, active low during transmission, open drain
27	DXA	O	Transmit data output for PCM Highway A (goes tristate when inactive)
28	DXB	O	Transmit data output for PCM Highway B (goes tristate when inactive)
29	$\overline{\text{TCB}}$	O	Transmit control output for PCM Highway B, active low during transmission, open drain

Table 1 Pin Definitions and Functions *SLICOFI-2x* (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
30	GNDPLL	Power	Digital ground PLL
31	VDDPLL	Power	+3.3 V supply voltage PLL
32	PCM/$\overline{\text{IOM-2}}$	I	PCM/$\overline{\text{IOM-2}}$ = 1: PCM/µC interface selected PCM/$\overline{\text{IOM-2}}$ = 0: IOM-2 interface selected
33	RSYNC	I	External ringing synchronization pin
34	$\overline{\text{RESET}}$	I	Reset pin, active low
35	TEST	I	Test pin for production test, has to be connected to GNDD
36	IO4A	I/O	User-programmable I/O Pin (Channel A) with analog input functionality
37	IO3A	I/O	User-programmable I/O Pin (Channel A) with analog input functionality
38	IO2A	I/O	User-programmable I/O Pin (Channel A) with relay-driving capability. SLICOFI-2 and SLIC-P: connected to pin C3 of SLIC-P, when two supply voltages for voice transmission and internal ringing are used.[1)]
39	IO1A	I/O	User-programmable I/O Pin (Channel A) with relay-driving capability. In external ringing mode, IO1 is used to automatically control and drive the ring relay.
40	GNDA	Power	Analog ground (Channel A)
41	VDDA	Power	+3.3 V analog supply voltage (Channel A)
42	ACNA	O	Differential two-wire AC output voltage controlling the TIP pin (Channel A)
43	ACPA	O	Differential two-wire AC output voltage controlling the RING pin (Channel A)
44	DCNA	O	Two-wire output voltage (DCN) (Channel A)
45	CDCNA	I/O	External capacitance for filtering (Channel A)
46	CDCPA	I/O	External capacitance for filtering (Channel A)
47	DCPA	O	Two-wire output voltage (DCP) (Channel A)
48	C2A	O	Ternary logic output for controlling the SLIC operation mode (Channel A)

Table 1 Pin Definitions and Functions *SLICOFI-2x* (cont'd)

Pin No.	Sym-bol	Input (I) Output (O)	Function
49	C1A	I/O	Ternary logic output, controlling the SLIC operation mode (Channel A); indicating thermal overload of SLIC if a current of typically 150 µA is drawn out
50	ILA	I	Longitudinal current input (Channel A)
51	ITACA	I	Transversal current input (AC) (Channel A)
52	ITA	I	Transversal current input (AC + DC) (Channel A)
53	VCMITA	I	Reference pin for trans./long. current sensing (Channel A)
54	VDDR	Power	+3.3 V analog supply voltage (bias)
55	GNDR	Power	Analog ground (bias)
56	VCMS	O	Reference voltage for differential two-wire interface, typical 1.5 V
57	VCM	O	Reference voltage for input pins IT, IL, ITAC
58	CREF	I/O	An external capacitor of 68 nF has to be connected to GNDR
59	SELCLK	I	Master clock select. Should be set to GND (internal master clock generation). For test purposes, external master clock generation can be selected (SELCLK = 1). In this case, a clock of nominal 32.768 MHz with a jitter time of less than 1 ns has to be applied to the MCLK pin.
60	VCMITB	I	Reference pin for transversal/longitudinal current sensing (Channel B)
61	ITB	I	Transversal current input (AC + DC) (Channel B)
62	ITACB	I	Transversal current input (AC) (Channel B)
63	ILB	I	Longitudinal current input (Channel B)
64	C1B	I/O	Ternary logic output, controlling the SLIC operation mode (Channel B); indicating thermal overload of SLIC if a current of typically 150 µA is drawn out

1) If SLIC-P is selected, IO2 cannot be controlled by the user, but is utilized by the SLICOFI-2 to control the C3 pin of the SLIC-P. Exception see **Table 9**.

2) "Wired-or" is not possible.

3 Functional Description

3.1 Functional Overview

3.1.1 Basic Functions of all *SLICOFI-2x* Codecs

The functions described in this section are integrated into all DuSLIC chip sets (see **Figure 3** for SLICOFI-2S and **Figure 4** for SLICOFI-2).

All BORSCHT functions are integrated:

- Battery feed
- Overvoltage protection
  (implemented by the robust high-voltage SLIC technology and additional circuitry)
- Ringing
- Signaling (supervision)
- Coding
- Hybrid for 2/4-wire conversion
- Testing

An important feature of the DuSLIC design is the fact that all the SLIC and codec functions are programmable via the IOM-2 or PCM/µC Interface of the dual-channel *SLICOFI-2x* device:

- DC (battery) feed characteristics
- AC impedance matching
- Transmit gain
- Receive gain
- Hybrid balance
- Frequency response in transmit and receive direction
- Ring frequency and amplitude
- Hook thresholds
- TTX modes

Because signal processing within the *SLICOFI-2x* is completely digital, it is possible to adapt to the requirements listed above by simply updating the coefficients that control DSP processing of all data. This means, for example, that changing impedance matching or hybrid balance requires no hardware modifications. A single hardware component is now capable of meeting the requirements for different markets. The digital nature of the filters and gain stages also assures high reliability, no drifts (over temperature or time) and minimal variations between different lines.

The characteristics for the two voice channels within *SLICOFI-2x* can be programmed independently of each other. The DuSLIC Coefficients Software (DuSLICOS) is provided to automate calculation of coefficients to match different requirements. DuSLICOS also verifies the calculated coefficients.

3.1.2 Additional Functions of the SLICOFI-2 Codec

The following line circuit functions are integrated only in the SLICOFI-2 codec (see **Figure 4**):

- Teletax metering

For pulse metering, a 12/16 kHz sinusoidal metering burst has to be transmitted. The DuSLIC chip set generates the metering signal internally and has an integrated notch filter.

- DTMF

DuSLIC has an integrated DTMF generator comprising two tone generators and one DTMF decoder. The decoder is able to monitor the transmit or receive path for valid tone pairs and outputs the corresponding digital code for each DTMF tone pair.

- Caller ID Frequency Shift Keying (FSK) Modulator

DuSLIC has an integrated FSK modulator capable of sending Caller ID information. The Caller ID modulator complies with all requirements of ITU-T recommendation V.23 and Bell 202.

- Line Echo Cancellation (LEC)

DuSLIC contains an adaptive Line Echo Cancellation unit for the cancellation of near end echos (up to 8 ms cancelable echo delay time).

- Universal Tone Detection (UTD)

DuSLIC has an integrated Universal Tone Detection unit to detect special tones in the receive or transmit path (for fax or modem tones).

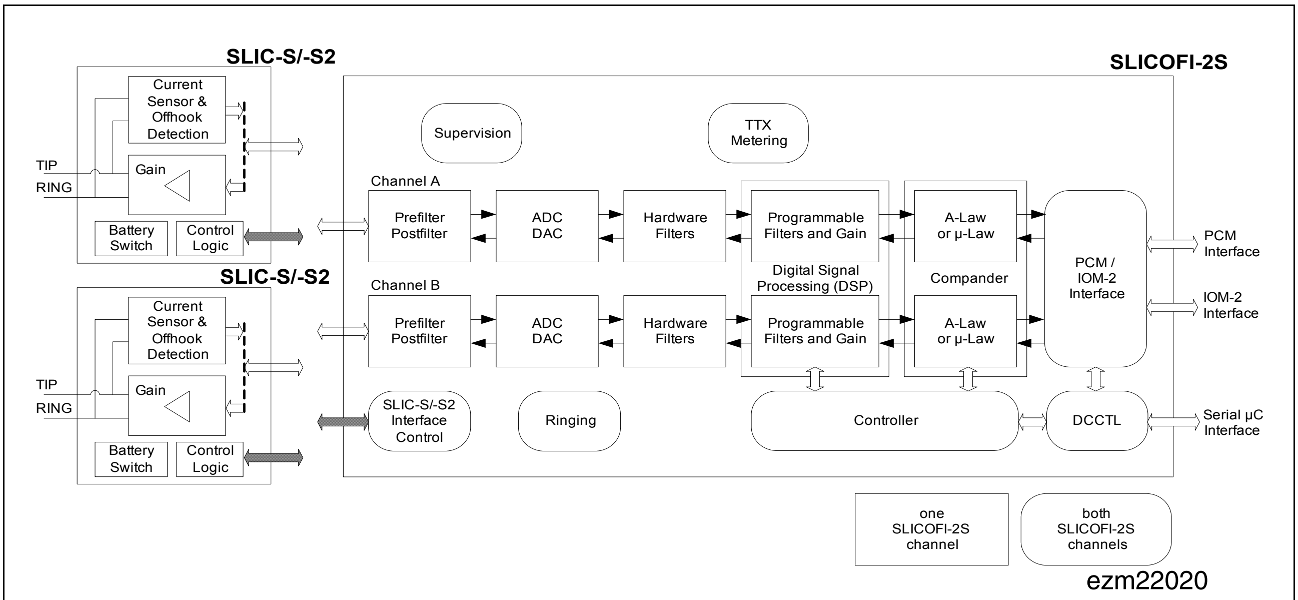


Figure 3 Line Circuit Functions in the SLICOFI-2S

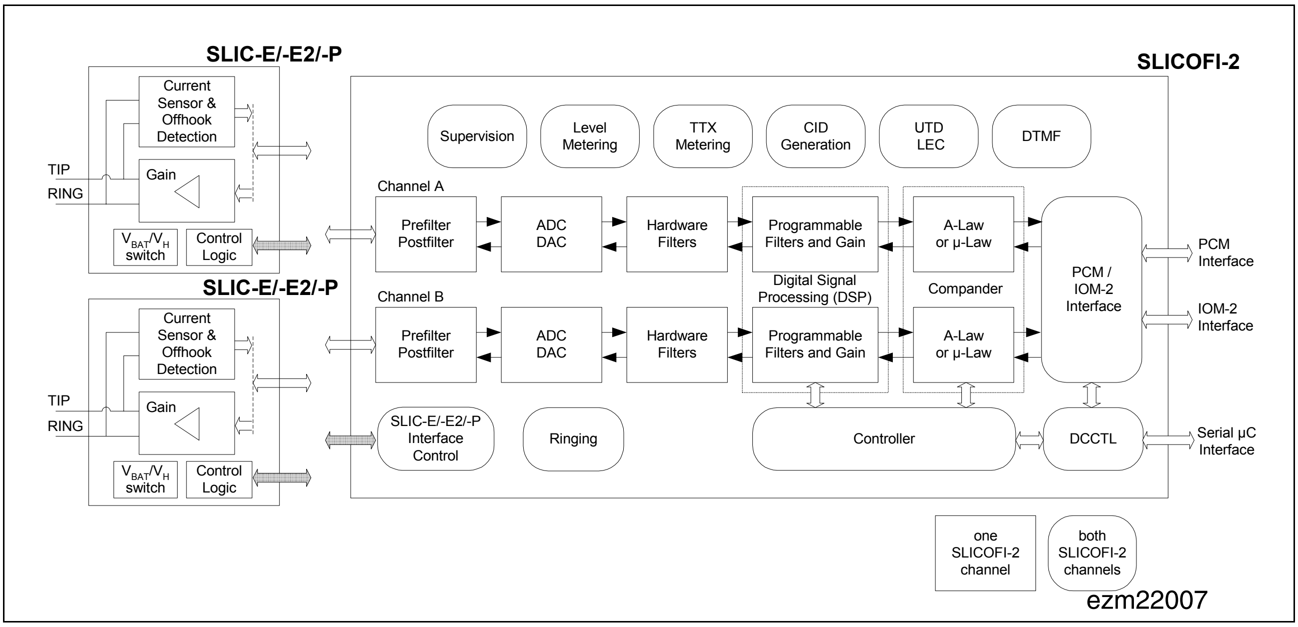


Figure 4 Line Circuit Functions in the SLICOFI-2

3.2 Block Diagrams

Figure 5 shows the internal block structure of all available *SLICOFI-2x* codec versions. The Enhanced Digital Signal Processor (EDSP) realizing the add-on funtions[1)] is only integrated in the SLICOFI-2 (PEB 3265) device.

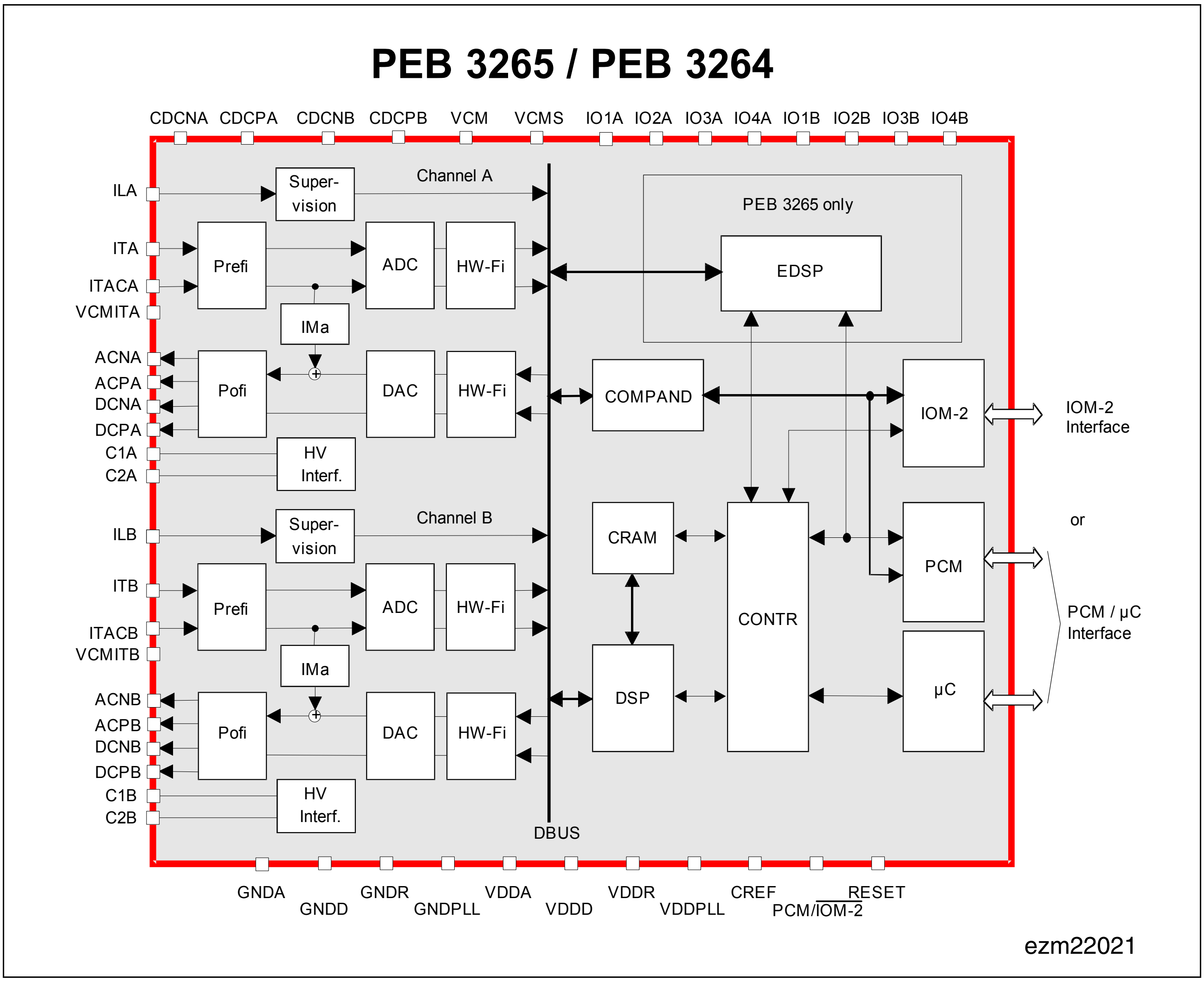


Figure 5 Block Diagram: *SLICOFI-2x* (PEB 3265, PEB 3264)

3.2.1 DTMF Generation

The *SLICOFI-2x* offers programmable DTMF generation for both channels by using the internal tone generators.

1) The add-on functions are DTMF detection, Caller ID generation, Message Waiting lamp support, Three-party Conferencing, Universal Tone Detection (UTD), Line Echo Cancellation (LEC), and Sleep Mode.

3.2.2 DTMF Detection in SLICOFI-2

Both channels A and B of the SLICOFI-2 have a powerful built-in DTMF decoder that will meet most national requirements. The receiver algorithm performance meets the quality criteria for central office/exchange applications. It complies with the requirements of ITU-T Q.24, Bellcore GR-30-CORE (TR-NWT-000506), and Deutsche Telekom network (BAPT 223 ZV 5, Approval Specification of the Federal Office for Post and Telecommunications, Germany), among others.

Note: DTMF Detection is only available with the SLICOFI-2 codec device.

The performance of the algorithm can be adapted according to the needs of the application via the digital interface (detection level, twist, bandwidth, and center frequency of the notch filter).

Table 2 shows the performance characteristics of the DTMF decoder algorithm:

Table 2 Performance Characteristics of the DTMF Decoder Algorithm

No.	Characteristic	Value	Notes
1	Valid input signal detection level	–48 to 0 dBm0	Programmable
2	Input signal rejection level	–5 dB of valid signal detection level	–
3	Positive twist accept	< 8 dB	Programmable
4	Negative twist accept	< 8 dB	Programmable
5	Frequency deviation accept	< ± (1.5% + 4 Hz) and < ± 1.8%	Related to center frequency
6	Frequency deviation reject	> ±3%	Related to center frequency
7	DTMF noise tolerance (could be the same as 14)	–12 dB	dB referenced to lowest amplitude tone
8	Minimum tone accept duration	40 ms	–
9	Maximum tone reject duration	25 ms	–
10	Signaling velocity	≥ 93 ms/digit	–
11	Minimum inter-digit pause duration	40 ms	–
12	Maximum tone drop-out duration	20 ms	–
13	Interference rejection 30 Hz to 480 Hz for valid DTMF recognition	Level in frequency range 30 Hz … 480 Hz ≤ level of DTMF frequency +22 dB	dB referenced to lowest amplitude tone

Table 2 Performance Characteristics of the DTMF Decoder Algorithm (cont'd)

No.	Characteristic	Value	Notes
14	Gaussian noise influence Signal level –22 dBm0, SNR = 23 dB	Error rate better than 1 in 10000	–
15	Pulse noise influence Impulse noise tape 201 according to Bellcore TR-TSY-000762	Error rate better than 14 in 10000	measured with DTMF level –22 dBm0 Impulse Noise –10 dBm0 and –12 dBm0

In the event of pauses < 20 ms:

- If the pause is followed by a tone pair with the same frequencies as before, this is interpreted as drop-out.
- If the pause is followed by a tone pair with different frequencies and if all other conditions are valid, this is interpreted as two different numbers.

DTMF decoders can be switched on or off individually to reduce power consumption. In normal operation, the decoder monitors the Tip and Ring wires via the ITAC pins (transmit path). Alternatively, the decoder can also be switched in the receive path. On detecting a valid DTMF tone pair, SLICOFI-2 generates an interrupt via the appropriate INT pin and indicates a change of status. The DTMF code information is provided by a register which is read via the digital interface.

The DTMF decoder also has excellent speech-rejection capabilities and complies with Bellcore TR-TSY-000763. The algorithm has been fully tested with the speech sample sequences in the Series-1 Digit Simulation Test Tapes for DTMF decoders from Bellcore.

3.2.3 Caller ID Generation in SLICOFI-2

The SLICOFI-2 contains a FSK generation unit for sending Caller ID information.

SLICOFI-2 FSK Generation

Different countries use different standards to send Caller ID information. The SLICOFI-2 chip is compatible with the widely used Bellcore GR-30-CORE, British Telecom (BT) SIN227, SIN242, and the UK Cable Communications Association (CCA) specification TW/P&E/312 standards. Continuous phase binary frequency shift keying (FSK) modulation is used for coding which is compatible with BELL 202 (see **Table 3**) and ITU-T V.23, the most common standards. The SLICOFI-2 can be easily adapted to these requirements by programming via the microcontroller interface. Coefficient sets are provided for the most common standards.

Table 3 FSK Modulation Characteristics

Characteristic	ITU-T V.23	Bell 202
Mark (Logic 1)	1300 ± 3 Hz	1200 ± 3 Hz
Space (Logic 0)	2100 ± 3 Hz	2200 ± 3 Hz
Modulation	FSK	
Transmission rate	1200 ± 6 baud	
Data format	Serial binary asynchronous	

3.2.4 Line Echo Cancelling (LEC) in SLICOFI-2

The SLICOFI-2 line echo canceller is compatible with applicable ITU-T G.165 and G.168 standards. An echo cancellation delay time of up to 8 ms can be programmed (for restrictions see chapter “MIPS requirements for EDSP Capabilities” in the DuSLIC Data Sheet).

4 Operating Modes for the DuSLIC Chip Set

Table 4 Operating Modes for *SLICOFI-2x* and SLICS

***SLICOFI-2x* Mode**	**SLIC Type**			**CIDD/CIOP [1]**			**Additional Bits used [2]**
	SLIC-S/ SLIC-S2	**SLIC-E/ SLIC-E2**	**SLIC-P**	**M2**	**M1**	**M0**	
Sleep (SL)	–	PDRH	PDRH	1	1	1	SLEEP-EN = 1
			PDRR	1	1	1	SLEEP-EN = 1, ACTR = 1
Power Down Resistive (PDR)	PDRH	PDRH	PDRH	1	1	1	SLEEP-EN = 0
			PDRR	1	1	1	SLEEP-EN = 0, ACTR = 1
Power Down High Impedance (PDH)	PDH	PDH	PDH	0	0	0	–
Active High (ACTH)	ACTH	ACTH	ACTH	0	1	0	–
Active Low (ACTL)	ACTL	ACTL	ACTL	0	1	0	ACTL = 1
Active Ring (ACTR)	ACTR	ACTR	ACTR	0	1	0	ACTR = 1
Ringing (Ring)	ACTR[3]	ACTR	ACTR	1	0	1	–
	–	–	ROT	1	0	1	HIT = 1
	–	–	ROR	1	0	1	HIR = 1
Active with HIT[4]	HIT	HIT		0	1	0	HIT = 1
			HIT	0	1	0	HIT = 1, ACTR = 0
Active with HIR[5]	HIR	HIR		0	1	0	HIR = 0
			HIR	0	1	0	HIR = 0, ACTR = 0
Active with Ring to Ground			ROT	0	1	0	HIT = 1, ACTR = 1
Active with Tip to Ground			ROR	0	1	0	HIR = 1, ACTR = 1
High Impedance on Ring and Tip (HIRT)	–	HIRT	HIRT	0	1	0	HIR = 1, HIT = 1

Table 4 Operating Modes for *SLICOFI-2x* and SLICS (cont'd)

***SLICOFI-2x* Mode**	**SLIC Type**			**CIDD/CIOP** [1)]			**Additional Bits used** [2)]
	SLIC-S/ SLIC-S2	**SLIC-E/ SLIC-E2**	**SLIC-P**	**M2**	**M1**	**M0**	
Active with Metering	ACTx[3)6)]	ACTx[4)]	ACTx[4)]	1	1	0	TTX-DIS to select Reverse Polarity or TTX Metering
Ground Start	HIT	HIT		1	0	0	–
			HIT	1	0	0	ACTR = 0
Ring Pause	ACTR[3)]	ACTR	ACTR ROR ROT	0	0	1	HIR = 1 HIT = 1

1) CIDD = Data Downstream Command/Indication Channel Byte (IOM-2 Interface)
CIOP = Command/Indication Operation
Fo further information, see *SLICOFI-2x Command Structure and Programming* in the DuSLC Data Sheet.

2) If not otherwise stated in the table, the bits ACTL, ACTR, HIT, HIR have to be set to 0.

3) Only for SLIC-S

4) HIT = High Impedance on Tip

5) HIR = High Impedance on Ring

6) ACTx means ACTH, ACTL or ACTR.

For a functional description of the operating modes see the DuSLIC Data Sheet.

4.1 SLICOFI-2S and SLIC-S/-S2 Interface

The SLIC-S/-S2 (PEB 4264/-2) operates in the following modes controlled by a ternary logic signal at the C1 and C2 input:

Table 5 SLIC-S/-S2 Interface Code

		C2		
		L	**M**	**H**
C1	**L**[1)]	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

1) No 'Overtemp' signaling possible via pin C1 if C1 is low.

Table 6 SLIC-S/-S2 Modes

SLIC-S/-S2 Mode	Mode Description	Internal Supply Voltages V_{BI}, V_{HI}
PDH	Power Down High Impedance	(supply switches open)
PDRH	Power Down Resistive High	(supply switches open)
PDRHL	Power Down Resistive High Load	(supply switches open)
ACTL	Active Low	V_{BATL}, BGND
ACTH	Active High	V_{BATH}, BGND
ACTR	Active Ring	V_{BATH}, V_{HR}
HIRT	High Impedance on RING and TIP	V_{BATH}, V_{HR}
HIT	High Impedance on TIP	V_{BATH}, V_{HR}
HIR	High Impedance on RING	V_{BATH}, V_{HR}

For the usage of the SLIC-S/-S2 modes see the SLIC-S/-S2 Data Sheet.

4.2 SLICOFI-2 and SLIC-E/-E2 Interface

The SLIC-E/-E2 (PEB 4265/-2) operates in the following modes controlled by ternary logic signals at C1, C2 and a binary signal at C3:

Table 7 SLIC-E/-E2 Interface Code

<table>
<tr><th colspan="2" rowspan="2"></th><th colspan="3">C2</th><th colspan="2" rowspan="2"></th></tr>
<tr><th>L</th><th>M</th><th>H</th></tr>
<tr><td rowspan="6">C1</td><td rowspan="2">L[1)]</td><td>PDH</td><td rowspan="2">PDRHL</td><td rowspan="2">PDRH</td><td>L or N.C.</td><td rowspan="6">C3</td></tr>
<tr><td>HIRT</td><td>H</td></tr>
<tr><td rowspan="2">M</td><td rowspan="2">ACTL</td><td rowspan="2">ACTH</td><td rowspan="2">ACTR</td><td>L or N.C.</td></tr>
<tr><td>H</td></tr>
<tr><td rowspan="2">H</td><td>HIRT</td><td rowspan="2">HIT</td><td rowspan="2">HIR</td><td>L or N.C.</td></tr>
<tr><td>ACTH-R</td><td>H</td></tr>
</table>

1) No ‘Overtemp’ signaling possible via pin C1 if C1 is low.

Table 8 SLIC-E/-E2 Modes

SLIC-E/-E2 Mode	Mode Description	Internal Supply Voltages V_{BI}, V_{HI}
PDH	Power Down High Impedance	Supply switches open
PDRH	Power Down Resistive High	Supply switches open
PDRHL	Power Down Resistive High Load	supply switches open
ACTL	Active Low	V_{BATL}, BGND
ACTH	Active High	V_{BATH}, BGND
ACTH-R	Active High Resistive	V_{BATH}, BGND
ACTR	Active Ring	V_{BATH}, V_{HR}
HIRT	High Impedance on RING and TIP	V_{BATH}, V_{HR}
HIT	High Impedance on TIP	V_{BATH}, V_{HR}
HIR	High Impedance on RING	V_{BATH}, V_{HR}

For the usage of the SLIC-E/-E2 modes see the SLIC-E/-E2 Data Sheet.

4.3 SLICOFI-2 and SLIC-P Interface

The SLIC-P (PEB 4266) operates in the following modes controlled by a ternary logic signal at the C1, C2 inputs and a binary logic signal at C3 input

Table 9 SLIC-P Interface Code

		C2				
		L	**M**	**H**		
C1	**L**[1]	PDH	PDRR	PDRRL	**L**	**C3**[2]
			PDRHL	PDRH	**H**	
	M	$ACTL_{90}$[3]	$ACTH_{90}$	$ACTR_{90}$	**L**	
		$ACTL_{60}$	$ACTH_{60}$	$ACTR_{60}$	**H**	
	H	HIRT	HIT	HIR	**L**	
			ROT	ROR	**H**	

1) No 'Overtemp' signaling possible via pin C1 if C1 is low.

2) The C3 pin of SLIC-P is typically connected to the IO2 pin of SLICOFI-2. It is recommended to use SEL-SLIC[1:0] = 10 in register BCR1. The IO2 pin (connected to the SLICs C3 pin) has to be programmed manually by the user according to the SLIC-P interface code table. It is recommended to use SEL-SLIC[1:0] = 10 in register BCR1. The IO2 pin (connected to the SLICs C3 pin) has to be programmed manually by the user according to the SLIC-P interface code table.

3) SLIC-P Version 1.2 features selectable current limitation (60 mA or 90 mA) in the Active and Ringing operating modes. In this document ACTL, ACTH and ACTR refers to both current limitation values.

Table 10 SLIC-P Modes

SLIC-P Mode	Mode Description	Internal Battery Supply Voltage
PDH	Power Down High Impedance	–
PDRH	Power Down Resistive High	V_{BATH}
PDRHL	Power Down Resistive High Load	V_{BATH}
PDRR	Power Down Resistive Ring	V_{BATR}
PDRRL	Power Down Resistive Ring Load	V_{BATR}
$ACTL_{90}$, $ACTL_{60}$	Active Low with Current Limitation 90 mA or 60 mA	V_{BATL}
$ACTH_{90}$, $ACTH_{60}$	Active High with Current Limitation 90 mA or 60 mA	V_{BATH}
$ACTR_{90}$, $ACTR_{60}$	Active Ring with Current Limitation 90 mA or 60 mA	V_{BATR}

Table 10 SLIC-P Modes (cont'd)

SLIC-P Mode	**Mode Description**	**Internal Battery Supply Voltage**
HIRT	High Impedance on RING and TIP	V_{BATR}
HIT	High Impedance on TIP (RING current limitation of 90 mA)	V_{BATR}
HIR	High Impedance on RING (TIP current limitation of 90 mA)	V_{BATR}
ROR	Ring on RING (current limitation 60 mA)	V_{BATR}
ROT	Ring on TIP (current limitation 60 mA)	V_{BATR}

For the usage of the SLIC-P modes see the SLIC-P Data Sheet.

5 Signal Path and Test Loops

The following figures show the main AC and DC signal path and the integrated analog and digital loops of the SLICOFI-2 and SLICOFI-2S.

Please note the interconnections between the AC and DC pictures of the respective chip set. For further information on the shown registers and bits/switches please see the DuSLIC Data Sheet.

5.1 AC Test Loops

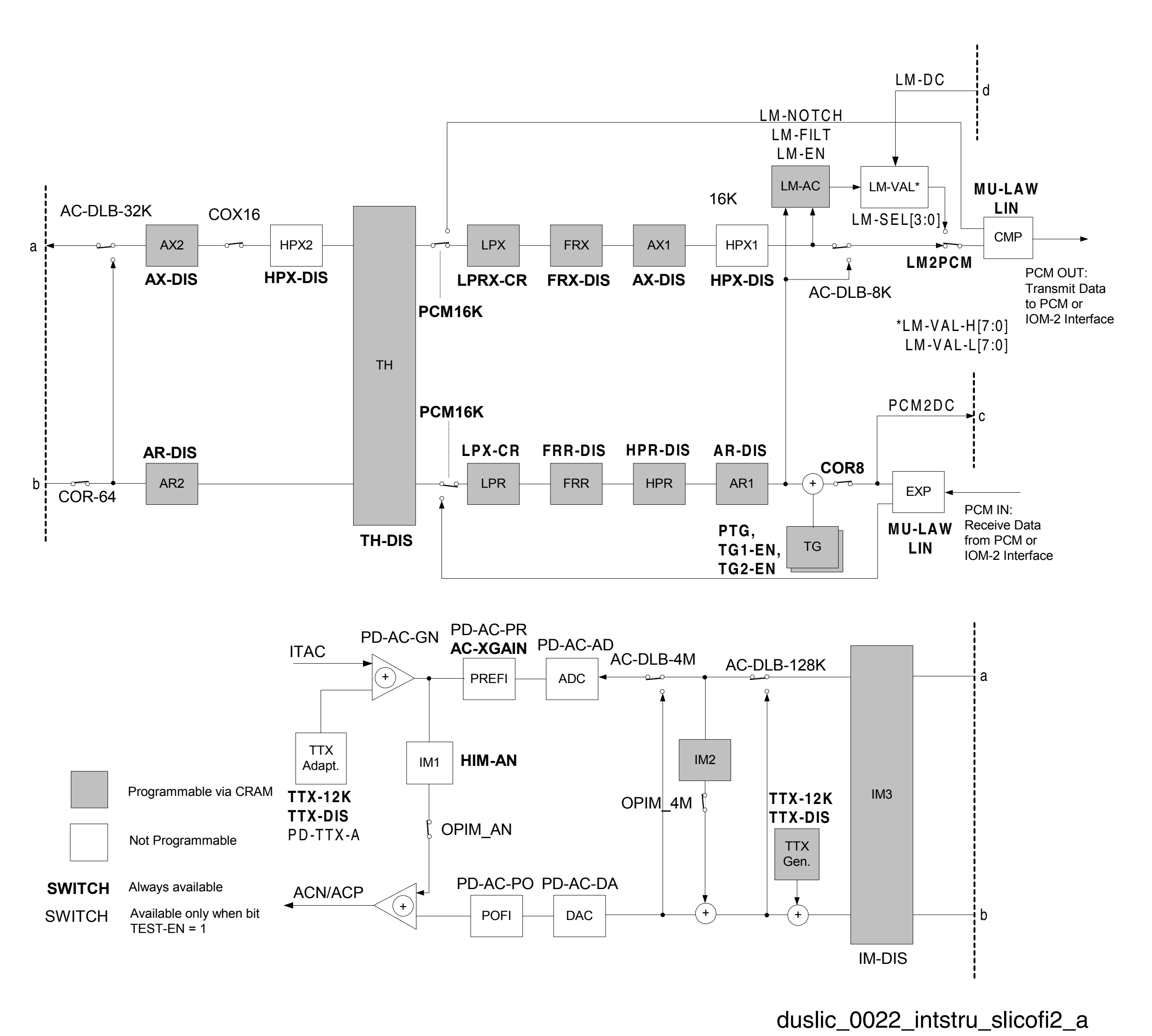


Figure 6 AC Test Loops SLICOFI-2

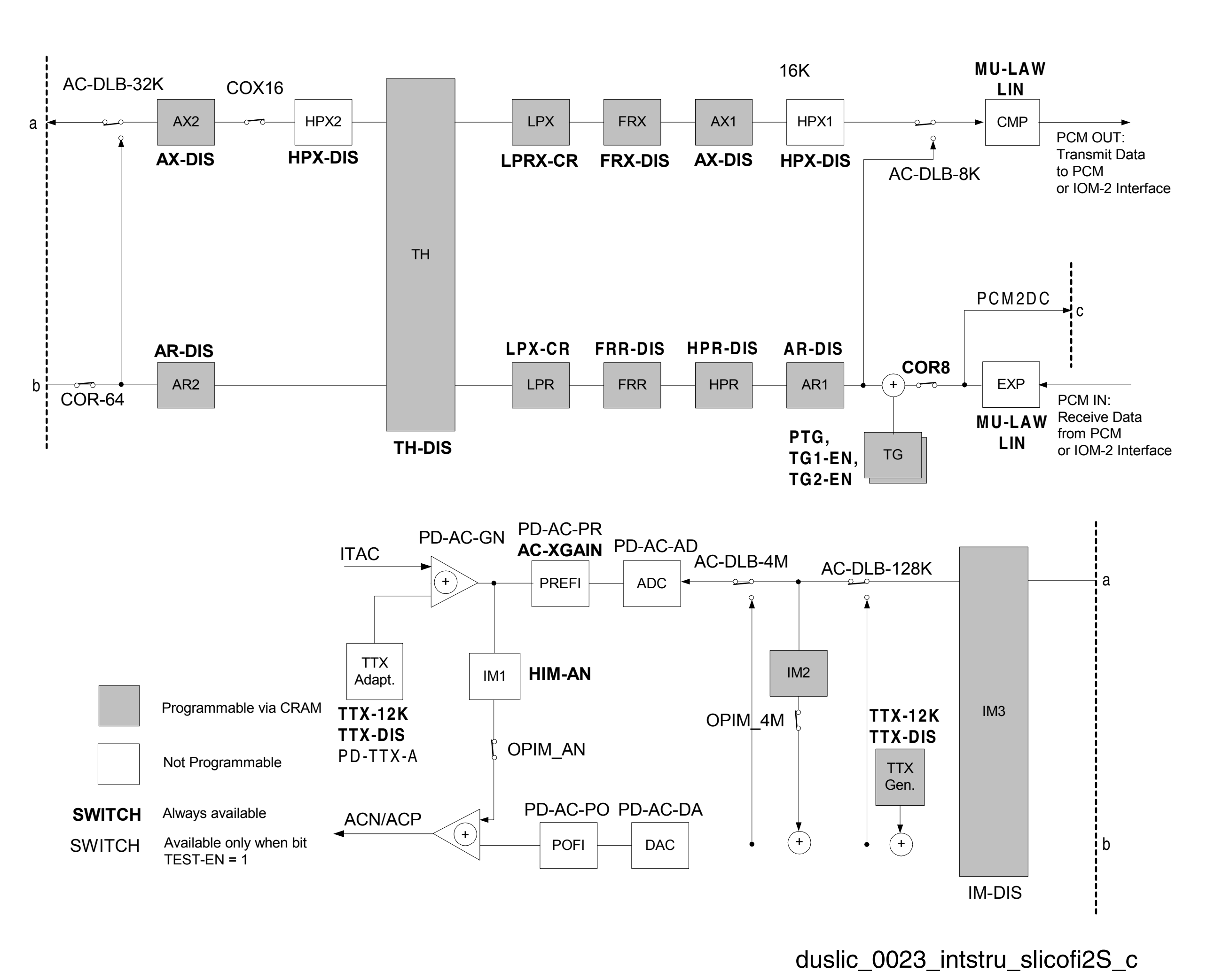


Figure 7 AC Test Loops SLICOFI-2S

5.2 DC Test Loops

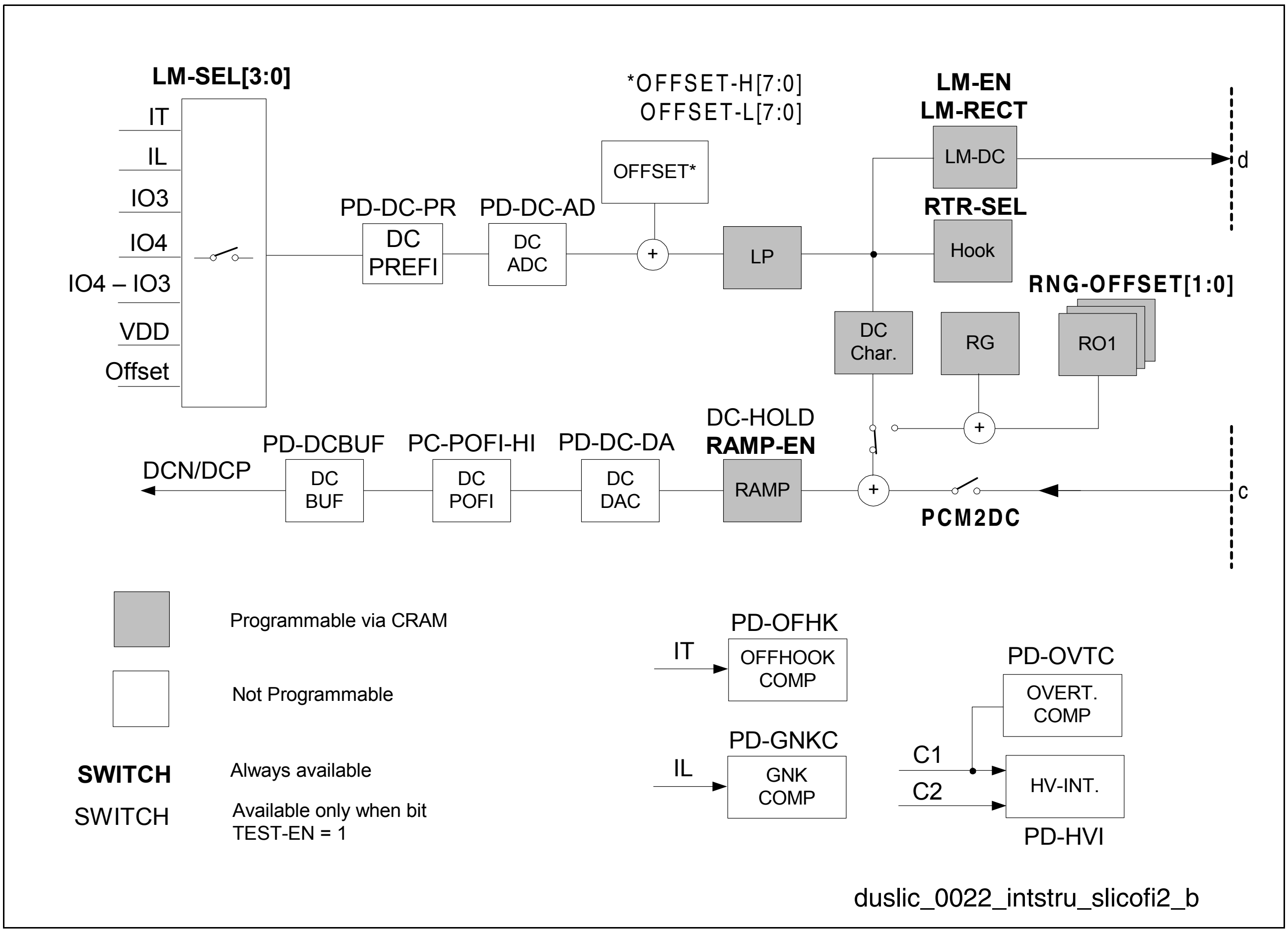


Figure 8 DC Test Loops SLICOFI-2 and SLICOFI-2S

6 Electrical Characteristics

6.1 Electrical Characteristics *SLICOFI-2x*

6.1.1 Absolute Maximum Ratings

Table 11 Absolute Maximum Ratings

Parameter[1)]	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Supply pins (VDDi) referred to corresponding ground pin (GNDi)	–	–0.3	4.6	V	–
Ground pins (GNDi) referred to any other ground pin (GNDj)	–	–0.3	0.3	V	–
Supply pins (VDDi) referred to any other supply pin (VDDj)	–	–0.3	0.3	V	–
Analog input and output pins	–	–0.3	3.6	V	V_{DDA} = 3.3 V, $V_{GNDA/B}$ = 0 V
Digital input and output pins	–	–0.3	5.5	V	V_{DDD} = 3.3 V, V_{GNDD} = 0 V
DC input and output current at any input or output pin (free from latch-up)	–	–	100	mA	–
Storage temperature	T_{STG}	–65	125	°C	–
Ambient temperature under bias	T_A	–40	85	°C	–
Power dissipation	P_D	–	1	W	–
ESD voltage	–	–	2	kV	Human body model[2)]
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model)[3)]

1) i, j = A, B, D, R, PLL

2) MIL STD 883D, method 3015.7 and ESD Assn. standard S5.1-1993.

3) EOS/ESD Assn. Standard DS5.3-1993.

Note: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional operation under these conditions is not guaranteed. Exposure to conditions beyond those indicated in the *recommended operational conditions of this specification may affect device reliability.*

6.1.2 Operating Range

$V_{GNDD} = V_{GNDPLL} = V_{GNDR} = V_{GNDA/B} = 0$ V

Table 12 Operating Range

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply pins (VDDi) referred to the corresponding ground pin (GNDi) (I = A, B, D, R, PLL)		3.135	3.3	3.465	V	
Analog input pins referred to the ground pin (GNDj) (j = A, B) IO3j, IO4j ITj, ILj, ITACj, VCMITj		0	–	3.3	V	V_{DDj} = 3.3 V V_{GNDj} = 0 V
Analog output pins referred to the ground pin (GNDj) (j = A, B) ACPj, DCPj, ACNj, DCNj, VCMS, VCM C1, C2		 0.3 1.3 0	 – – –	 2.7 1.7 3.3	 V V V	V_{DDj} = 3.3 V V_{GNDj} = 0 V
Analog pins for passive devices to ground pin (GNDj) (j = A, B) CDCPj, CDCNj CREF		 0 1.3	 – –	 3.3 1.7	 V V	V_{DDj} = 3.3 V V_{GNDj} = 0 V
Digital input and output pins		0	–	5	V	
Ambient temperature	T_A	–40	–	+85	°C	

6.1.3 Power Up Sequence

The power up of VDDA, VDDB, VDDR, VDDD and VDDPLL should be performed simultaneously. No voltage should be supplied to any input or output pin before the VDD voltages are applied.

6.1.4 Power Dissipation SLICOFI-2

T_A = –40 °C to 85 °C, unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{DDB} = V_{DDR} = V_{DDPLL}$ = 3.3 V ±5 %;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL}$ = 0 V

Table 13 Power Dissipation SLICOFI-2

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current [1]						
Sleep both channels	$I_{DDSleep}$	–	5	7	mA	(MCLK, PCLK = 2 MHz)
Power Down both channels	$I_{DDPDown}$	–	24	30	mA	–
Active one channel	I_{DDAct1}	–	39	46	mA	without EDSP[2]
		–	43	50	mA	with 8 MIPS (DTMF detection)
		–	47	55	mA	with 16 MIPS
Active both channels	I_{DDAct2}	–	55	70	mA	without EDSP
		–	70	90	mA	with 32 MIPS
Power dissipation[1]						
Sleep both channels	$P_{DDSleep}$	–	17	25	mW	(MCLK, PCLK = 2 MHz)
Power Down both channels	$P_{DDPDown}$	–	79	104	mW	–
Active one channel	P_{DDAct1}	–	129	160	mW	without EDSP
		–	142	174	mW	with 8 MIPS (DTMF detection)
		–	155	191	mW	with 16 MIPS
Active both channels	P_{DDAct2}	–	182	243	mW	without EDSP
		–	231	315	mW	with 32 MIPS

1) Power dissipation and supply currents are target values

2) EDSP features are DTMF detection, Caller ID generation, Line Echo Cancellation (LEC), and Universal Tone Detection (UTD).

6.1.5 Power Dissipation SLICOFI-2S

T_A = –40 °C to 85 °C, unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{DDB} = V_{DDR} = V_{DDPLL}$ = 3.3 V ±5 %;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL}$ = 0 V

Table 14 Power Dissipation SLICOFI-2S

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current [1]						
Power Down both channels	$I_{DDPDown}$	–	24	30	mA	–
Active one channel	I_{DDAct1}	–	39	46	mA	–
Active both channels	I_{DDAct2}	–	55	70	mA	–
Power dissipation[1]						
Power Down both channels	$P_{DDPDown}$	–	79	104	mW	–
Active one channel	P_{DDAct1}	–	129	160	mW	–
Active both channels	P_{DDAct2}	–	182	243	mW	–

1) Power dissipation and supply currents are target values

6.1.6 Digital Interface

T_A = –40 to +85 °C, unless otherwise stated.

$V_{DD} = V_{DDD} = V_{DDA/B}$ = 3.3 V ±5%; $V_{GNDD} = V_{GNDA/B}$ = 0 V

Table 15 Digital Interface

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
For all input pins (including IO pins):						
Low-input pos.-going	V_{T+}	–	1.70	1.82	V	see Figure 9
High-input neg.-going	V_{T-}	1.13	1.20	–	V	see Figure 9
Input hysteresis	V_H	0.48	0.5	0.56	V	$V_H = V_{T+} - V_{T-}$
Spike rejection for reset	t_{rej}	1	–	4	µs	–

Table 15 Digital Interface (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
For all output pins except DU, DXA, DXB, IO1, IO2 (including IO pins):						
Low-output voltage	V_{OL}	–	0.35	0.4	V	I_O = –3.6 mA
High-output voltage	V_{OH}	2.7	3.0	–	V	I_O = 3.3 mA
for pins DU, DXA, DXB						
Low-output voltage	V_{OLDU}	–	0.35	0.4	V	I_O = –6 mA
High-output voltage	V_{OHDU}	2.7	3.0	–	V	I_O = 5.3 µA
for pins IO1, IO2						
Low-output voltage	V_{OLDU}	–	0.35	0.4	V	I_O = –50 mA (SLICOFI-2)
	V_{OLDU}	–	0.35	0.4	V	I_O = –30 mA (SLICOFI-2S)
High-output voltage	V_{OHDU}	2.7	3.0	–	V	I_O = 3.3 µA

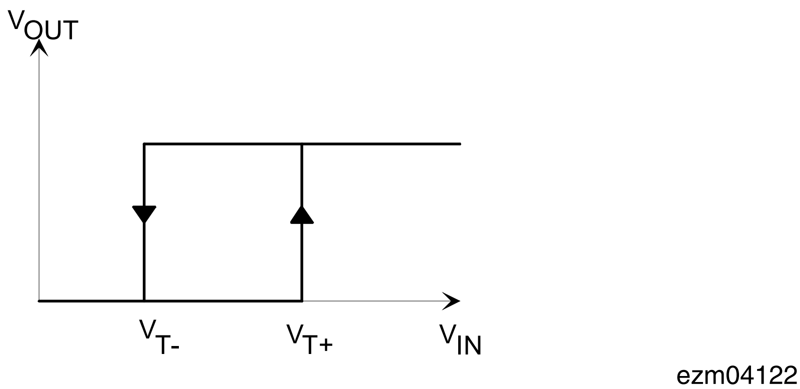


Figure 9 Hysteresis for Input Pins

6.1.7 Miscellaneous Characteristics

T_A = –40 °C to 85 °C, unless otherwise stated.

Table 16 Miscellaneous Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Leakage						
all digital input and input/output pins all analog input pins	I_L	–3	–	3	µA	–
Comparator Thresholds						
Off Hook comparator						V_{DD} = 3.3 V
threshold	V_{THRESH}	–	V_{CM} – 0.275	–	V	
GNDkey comparator						
positive threshold	$V_{THRESH+}$	–	V_{CM} + 0.275	–	V	
negative threshold	$V_{THRESH-}$	–	V_{CM} – 0.275	–	V	
threshold hysteresis	$V_{THR\text{-}hyst.}$	–	0.045	–	V	
SLIC Overtemperature Comparator at Pins C1						
Overtemperature comparator	I_{OTLo}		–	30	µA	Normal Operation
	I_{OTHi}	120		200		Overtemp. detected

6.2 AC Transmission *SLICOFI-2x*

The specification is based on the subscriber linecard requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires the consideration of the complete analog environment of the *SLICOFI-2x* device.

Functionality and performance are guaranteed for T_A = 0 to 70 °C by production testing. Extented temperature range operation at –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

Test Conditions

T_A = –40 °C to 85 °C, unless otherwise stated.

$V_{DDD} = V_{DDA} = V_{DDB} = V_{DDR} = V_{DDPLL}$ = 3.3 V ±5 %;

$V_{GNDA} = V_{GNDB} = V_{GNDR} = V_{GNDD} = V_{GNDPLL}$ = 0 V

Register BCR4: TH-DIS = 1, IM-DIS = 1, AX-DIS = 1, AR-DIS = 1

Register LMCR2: TEST-EN = 1

Register TSTR4: OPIM-AN = 1, OPIM-4M = 1

If not otherwise stated, the default settings are used.

The 0 dBm0 definitions for receive and transmit are:

A 0 dBm0 AC signal in transmit direction is equivalent to 0.5911 Vrms measured at pins ITACi/VCMITi (i = A, B).

A 0 dBm0 AC signal in receive direction is equivalent to 0.5911 Vrms measured at pins ITACi/VCMITi (i = A, B).

Table 17 AC Transmission

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Insertion Loss						
A-D (see Figure 11)	PCM_{OUT}	V_G = –11.88 dBm0 f = 1015.625 Hz	–0.2	0	+0.2	dBm0
D-A (see Figure 11)	V_{AC}	PCM_{in} = 0 dBm0 f = 1015.625 Hz	–2.668	–2.868	–3.068	dBm0

Table 17 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Frequency Response						
Receive loss Frequency variation	G_{RAF}	Reference frequency 1014 Hz, signal level 0 dBm0, H_{FRR} = 1				
		f = 300 Hz	–0.17	0.03	0.23	dB
		f = 2400 Hz	–0.08	0.12	0.32	dB
		f = 3000 Hz	–0.04	0.16	0.36	dB
Transmit loss Frequency variation	G_{XAF}	Reference frequency 1014 Hz, signal level 0 dBm0, H_{FRX} = 1				
		f = 300 Hz	–0.16	0.04	0.24	dB
		f = 2400 Hz	–0.15	0.05	0.25	dB
		f = 3000 Hz	–0.14	0.06	0.26	dB
Gain Tracking (see Figure 12 and Figure 13)						
Transmit gain Signal level variation	G_{XAL}	Sinusoidal test method f = 1014 Hz, reference level 0 dBm0				
		VF_XI = –55 to –50 dBm0	–1.4	–	1.4	dB
		VF_XI = –50 to –40 dBm0	–0.5	–	0.5	dB
		VF_XI = –40 to +3 dBm0	–0.25	–	0.25	dB
Receive gain Signal level variation	G_{RAL}	Sinusoidal test method f = 1014 Hz, reference level 0 dBm0				
		D_R0 = –55 to –50 dBm0	–1.4	–	1.4	dB
		D_R0 = –50 to –40 dBm0	–0.5	–	0.5	dB
		D_R0 = –40 to +3 dBm0	–0.25	–	0.25	dB

Table 17 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Group Delay (see Figure 14)						
Transmit delay, absolute	D_{XA}	f = 500 - 2800 Hz	400	490	585	µs
Receive delay, absolute	D_{RA}	f = 500 - 2800 Hz	290	380	475	µs
Group delay distortion, Receive and Transmit, relative to 1500 Hz, (see Figure 14)	D_{XR}					
		f = 500 - 600 Hz	–	–	300	µs
		f = 600 - 1000 Hz	–	–	150	µs
		f = 1000 - 2600 Hz	–	–	100	µs
		f = 2600 - 2800 Hz	–	–	150	µs
		f = 2800 - 3000 Hz	–	–	300	µs
Overload compression A/D (see Figure 10)						
Total Harmonic Distortion						
Transmit	THD4	–7 dBm0, 300 - 3400 Hz	–	–50	– 44	dB
Receive	THD2	–7 dBm0, 300 - 3400 Hz	–	–50	– 44	dB
Idle Channel Noise						
at ACN, ACP (receive) A-Law	N_{RP}	Psophometric	–	–103	–92	dBmp
PCM side (transmit) A-Law	N_{TP}	Psophometric	–	–84	–75	dBmp

Table 17 AC Transmission (cont'd)

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Distortion (Sinusoidal Test Method)						
Signal to total distortion Transmit	STD_X	f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law)				
		Add –45 dBm0	27	29.7	–	dB
		Add –40 dBm0	32	35	–	dB
		Add 0 dBm0	36.5	41	–	dB
Signal to total distortion Receive	STD_R	f = 1014 Hz (C message-weighted for µ-Law, psophometrically weighted for A-Law)				
		Add –45 dBm0	22	25	–	dB
		Add –40 dBm0	29	32	–	dB
		Add 0 dBm0	36.5	40	–	dB
Power Supply Rejection Ratio						
Power supply rejection ratio	PSRR	ripple: 1 kHz, 70 mVrms	–	–	–	–
Receive V_{DD}	–	at DCP/DCN at ACP/ACN	48	70	–	dB
Transmit V_{DD}	–	at IOM-2 / PCM	32	70	–	dB
Crosstalk						
Same channel	–	0 dBm0, 1014 Hz				
TX or RX	–		–	–	–75	dBm0
RX to TX	–		–	–	–75	dBm0
Between channels	–	0 dBm0, 1014 Hz				
TX or RX to TX	–		–	–	–75	dBm0
TX or RX to RX	–		–	–	–75	dBm0

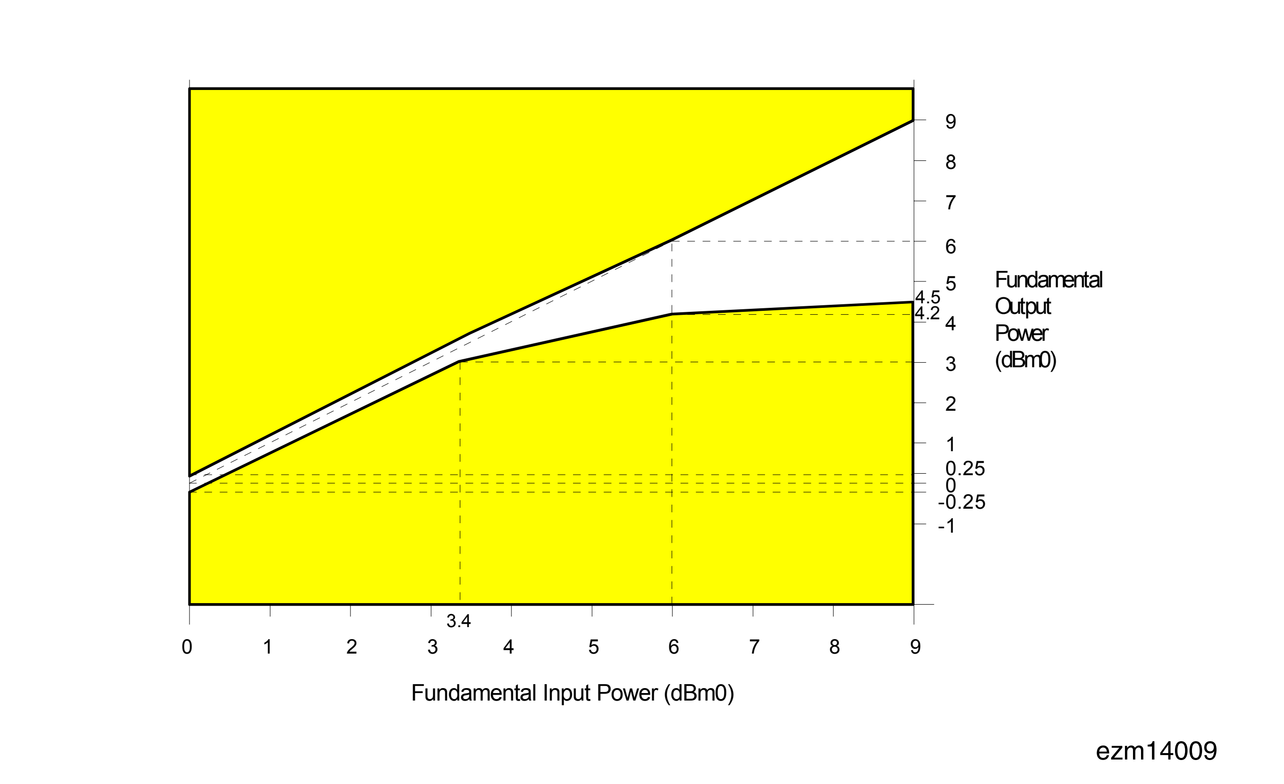


Figure 10 Overload Compression A/D

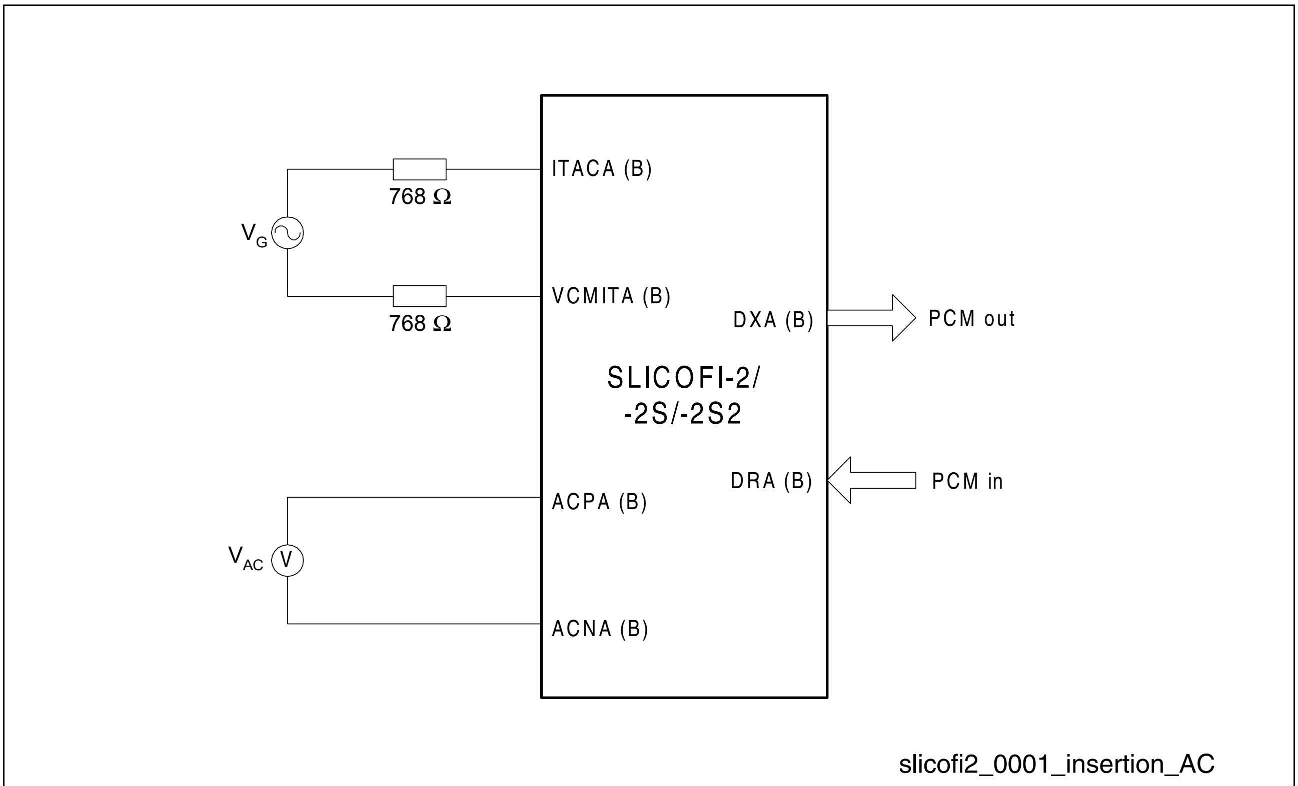


Figure 11 Insertion Loss

6.2.1 Gain Tracking (Receive or Transmit)

The gain deviations stay within the limits in the figures below.

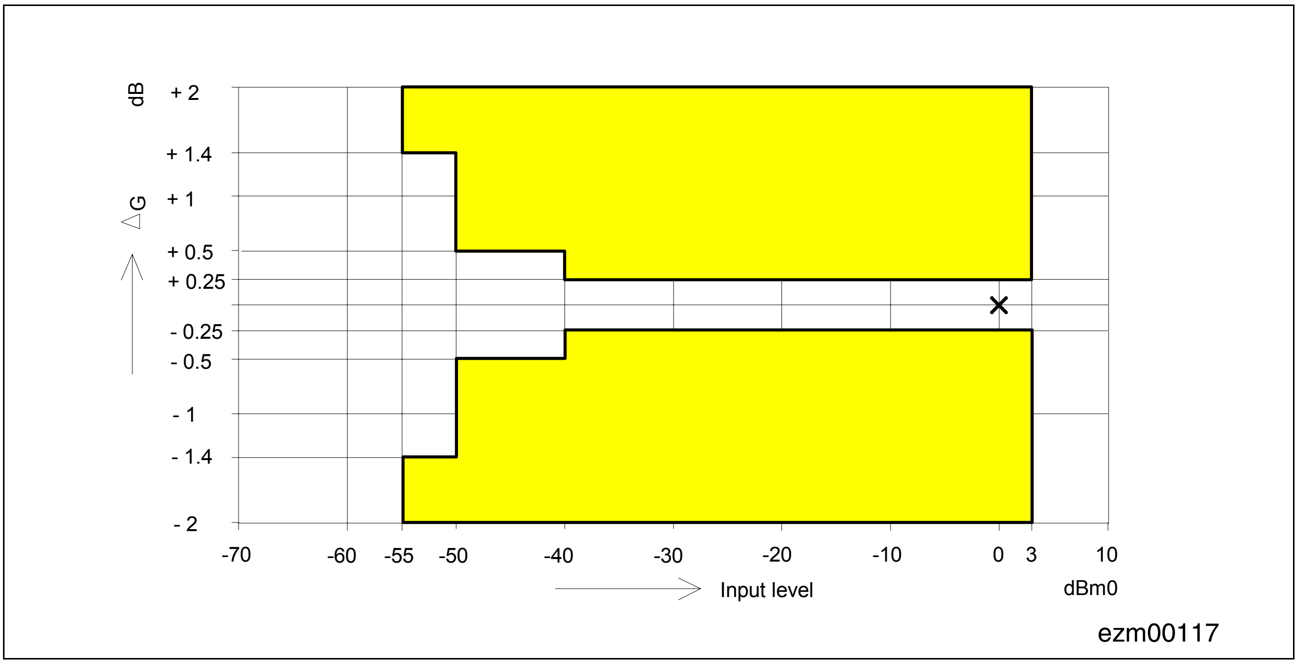


Figure 12 Gain Tracking Receive

Measured with a sine wave of f = 1014 Hz, reference level is –0 dBm0

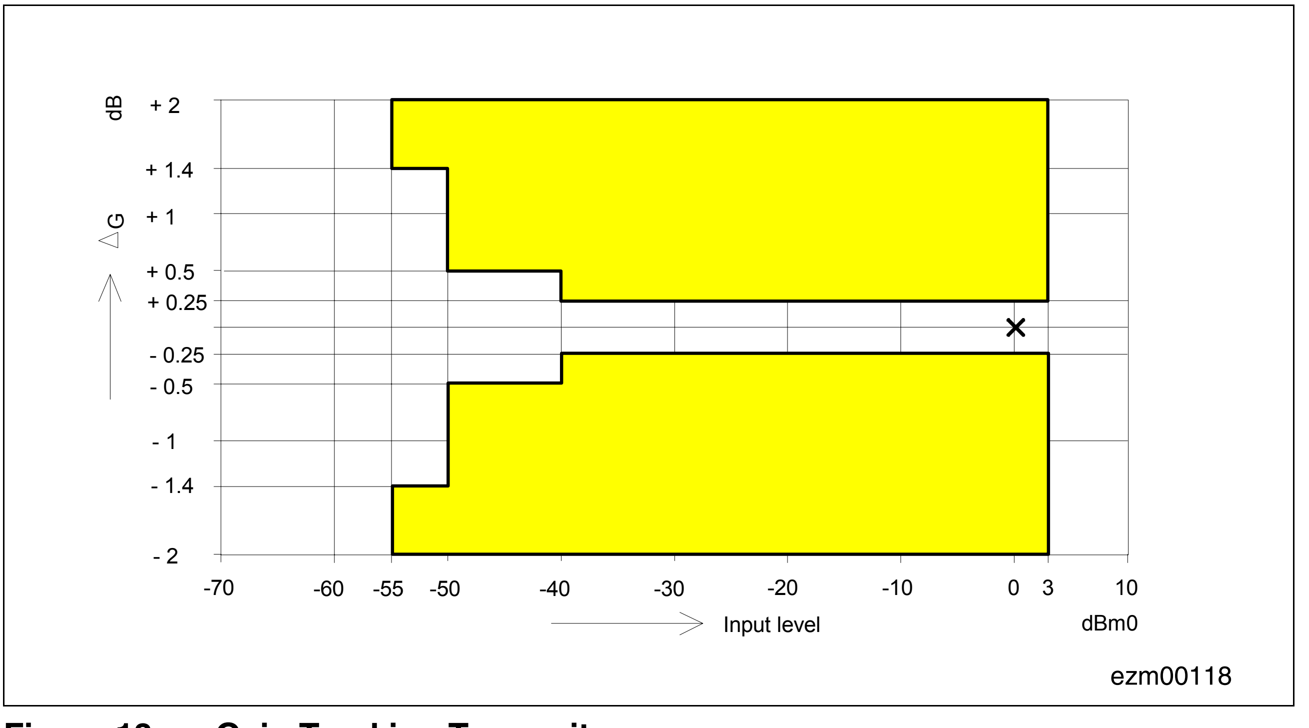


Figure 13 Gain Tracking Transmit

Measured with a sine wave of f = 1014 Hz, reference level is –0 dBm0

6.2.2 Group Delay

Minimum delays occure when the *SLICOFI-2x* is operating with disabled Frequency Response Receive and Transmit filters including the delay through A/D and D/A converters. Specific filter programming may cause additional group delays. Absolute Group delay also depends on the programmed time slot.

Group delay deviations stay within the limits in the figures below.

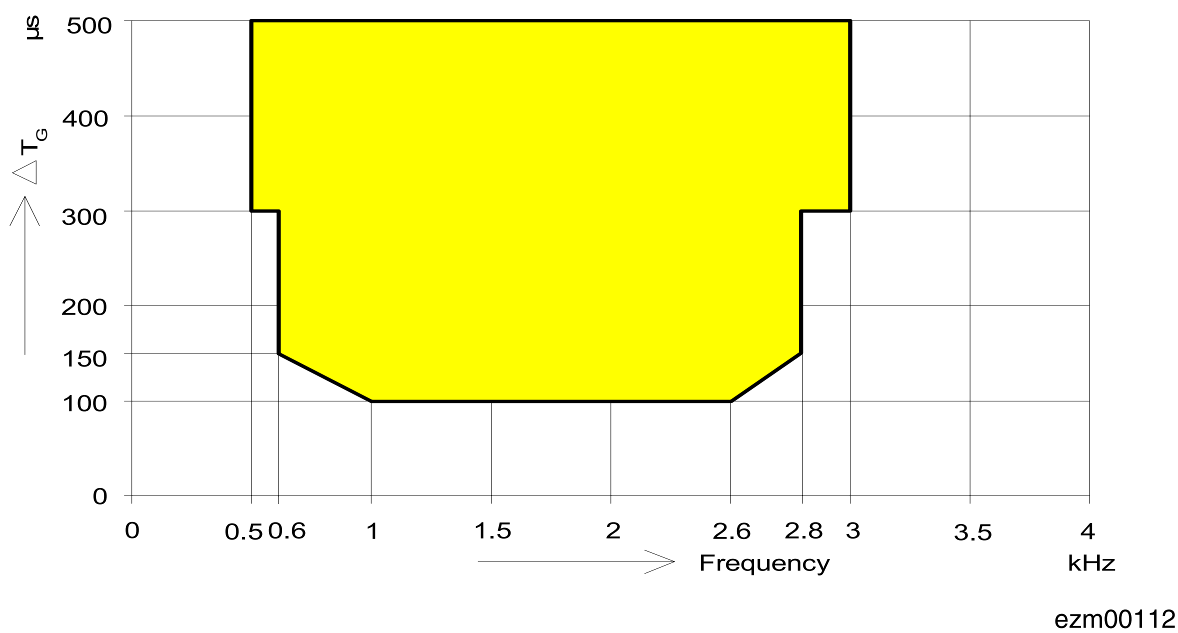


Figure 14 Group Delay Distortion Receive and Transmit

Signal level 0 dBm0

6.3 DC Characteristics *SLICOFI-2x*

T_A = –40 °C to 85 °C, unless otherwise stated.

Table 18 DC Characteristics *SLICOFI-2x*

Parameter	Symbol	Conditions	Limit Values			Unit
			min.	typ.	max.	
Insertion Loss						
A-D (see **Figure 15**)	PCM_{OUT}	V_G = 0.728 dBm0 A-Law, Bits LMSEL[3:0] = 0101 (register LMCR2) Bit LM2PCM = 1 (register LMCR1) f = 296.875 Hz	–0.2	0	+0.2	dBm0
D-A (see **Figure 15**)	V_{AC}	PCM_{in} = 0 dBm0 Bit PCM2DC = 1 (register LMCR1) Bit RNG-OFFSET[1:0] = 10 (register LMCR3) f = 296.875 Hz	5.775	5.975	6.175	dBm0

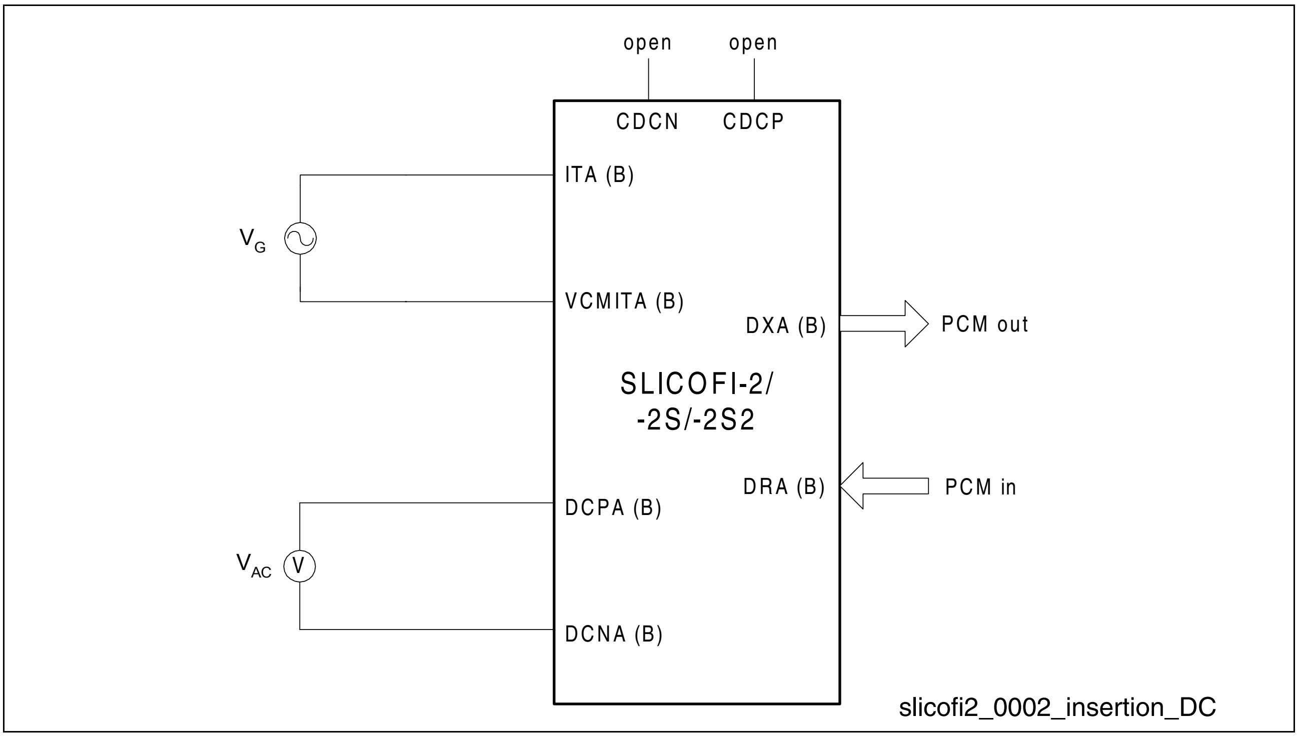


Figure 15 Insertion Loss

6.4 Timing Characteristics *SLICOFI-2x*

T_A = –40 °C to 85 °C, unless otherwise stated.

6.4.1 Input/Output Waveform for AC Tests

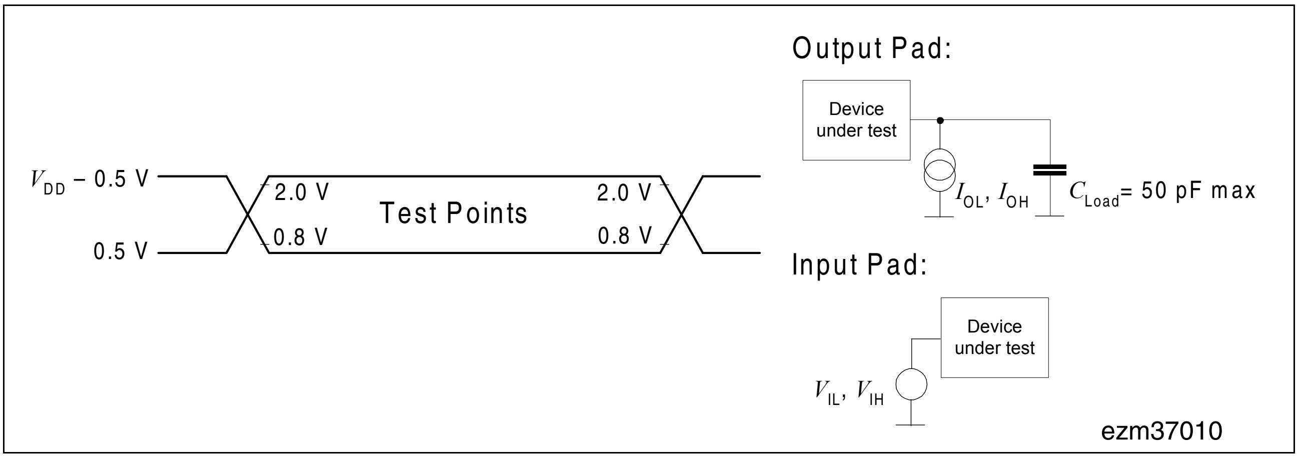


Figure 16 Waveform for AC Tests

During AC-Testing, the CMOS inputs are driven at a low level of 0.8 V and a high level of 2.0 V. The CMOS outputs are measured at 0.5 V and V_{DD} – 0.5 V respectively.

6.4.2 MCLK/FSC Timing

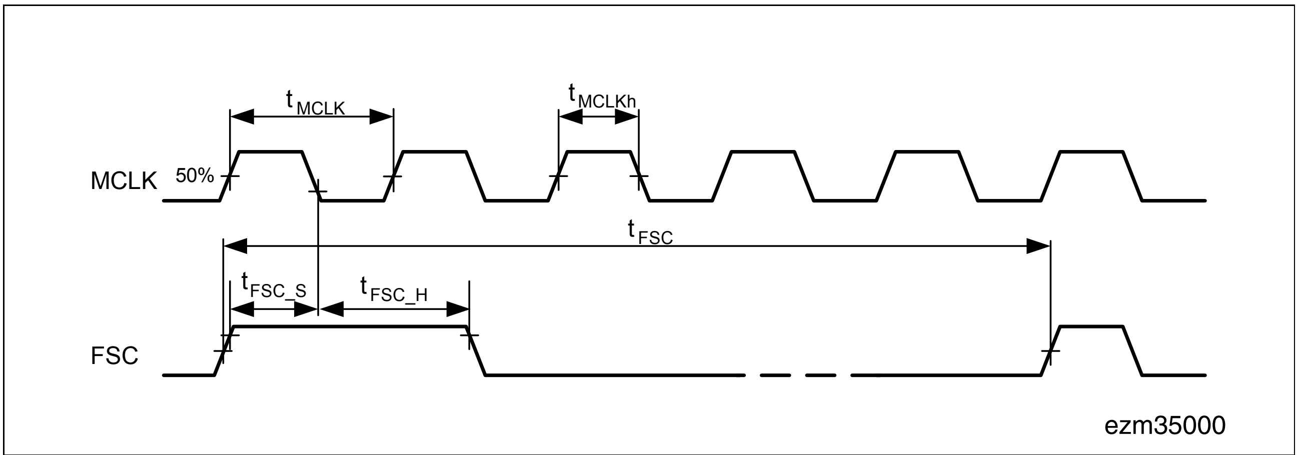


Figure 17 MCLK / FSC-Timing

Table 19 MCLK / FSC-Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period MCLK[1]	t_{MCLK}				ns
512 kHz ± 100 ppM		1952.93	1953.13	1953.32	
1536 kHz ± 100 ppM		650.98	651.04	651.11	
2048 kHz ± 100 ppM		488.23	488.28	488.33	
4096 kHz ± 100 ppM		244.116	244.141	244.165	
7168 kHz ± 100 ppM		139.495	139.509	139.523	
8192 kHz ± 100 ppM		122.058	122.070	122.082	
MCLK high time	t_{MCLKh}	$0.4 \times t_{MCLK}$	$0.5 \times t_{MCLK}$	$0.6 \times t_{MCLK}$	ns
Period FSC[1]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time	t_{FSC_h}	40	50	–	ns
FSC (or PCM) jitter time		$-0.2 \times t_{MCLK}$		$+0.2 \times t_{MCLK}$	ns

1) The MCLK frequency must be an integer multiple of the FSC frequency.

6.4.3 PCM Interface Timing

6.4.3.1 Single-Clocking Mode

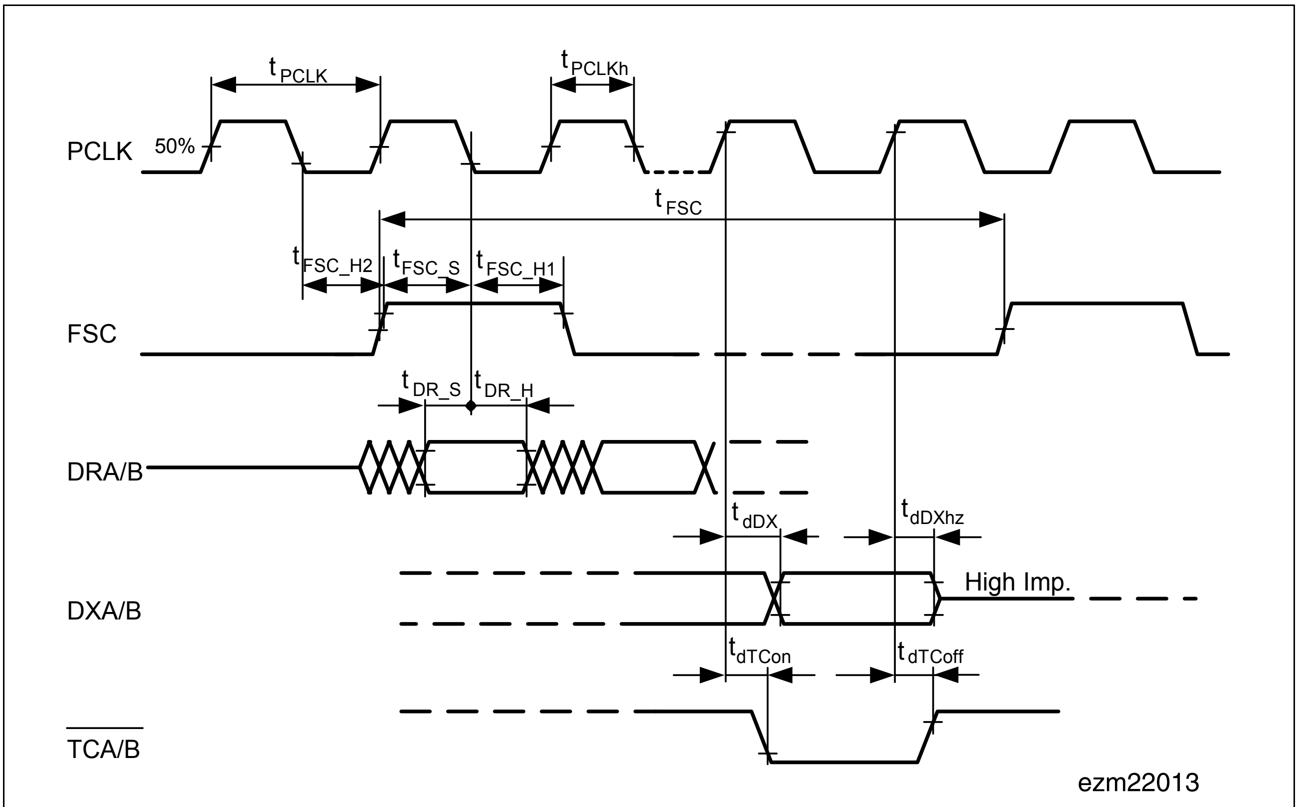


Figure 18 PCM Interface Timing – Single-Clocking Mode

Table 20 PCM Interface Timing – Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK[1)]	t_{PCLK}	1/8192	1/(n*64) with $2 \leq n \leq 128$	1/128	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	$0.5 \times t_{PCLK}$	$0.6 \times t_{PCLK}$	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{PCLK} - t_{FSC\_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DRA/B setup time	t_{DR_s}	10	50	–	ns
DRA/B hold time	t_{DR_h}	10	50	–	ns

Table 20 PCM Interface Timing – Single-Clocking Mode (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DXA/B delay time[2]	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] $\times$ C_{Load}[pF]	ns
DXA/B delay time to high Z	t_{dDXhz}	25	–	50	ns
TCA/B delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] $\times$ C_{Load}[pF]	ns
TCA/B delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + 2 $\times$ R_{Pullup}[kΩ] $\times$ C_{Load}[pF])	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency.

2) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

6.4.3.2 Double-Clocking Mode

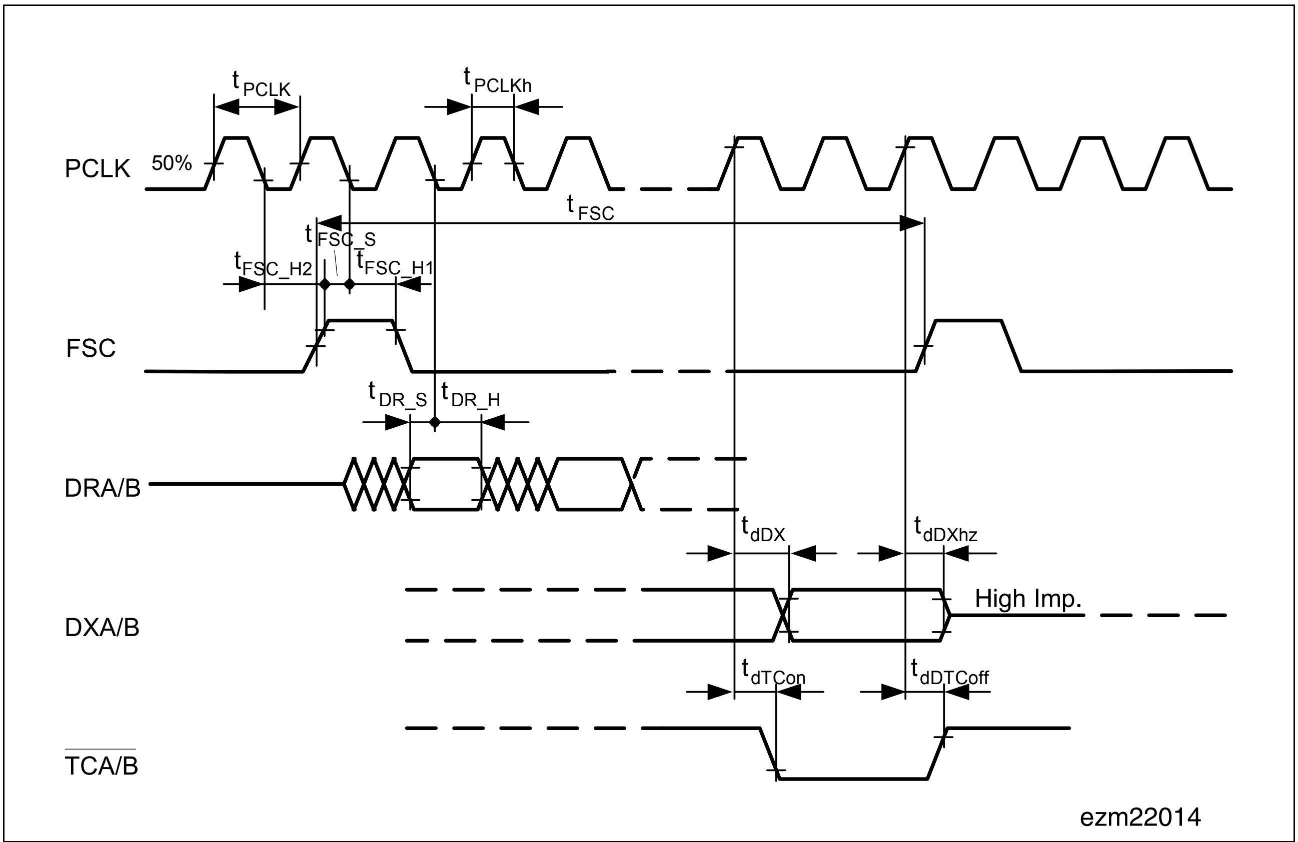


Figure 19 PCM Interface Timing – Double-Clocking Mode

Table 21 PCM Interface Timing – Double-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period PCLK[1]	t_{PCLK}	1/8192	1/(n*64) with $4 \leq n \leq 128$	1/256	ms
PCLK high time	t_{PCLKh}	$0.4 \times t_{PCLK}$	$0.5 \times t_{PCLK}$	$0.6 \times t_{PCLK}$	µs
Period FSC[1]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{PCLK} - t_{FSC\_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DRA/B setup time	t_{DR_s}	10	50	–	ns
DRA/B hold time	t_{DR_h}	10	50	–	ns
DXA/B delay time[2]	t_{dDX}	25	–	t_{dDX_min} + 0.4[ns/pF] $\times$ C_{Load}[pF]	ns
DXA/B delay time to high Z	t_{dDXhz}	25	–	50	ns
TCA/B delay time on	t_{dTCon}	25	–	t_{dTCon_min} + 0.4[ns/pF] $\times$ C_{Load}[pF]	ns
TCA/B delay time off	t_{dTCoff}	25	–	t_{dTCoff_min} + $2 \times R_{Pullup}$[kΩ] $\times C_{Load}$[pF])	ns

1) The PCLK frequency must be an integer multiple of the FSC frequency.

2) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

6.4.4 Microcontroller Interface Timing

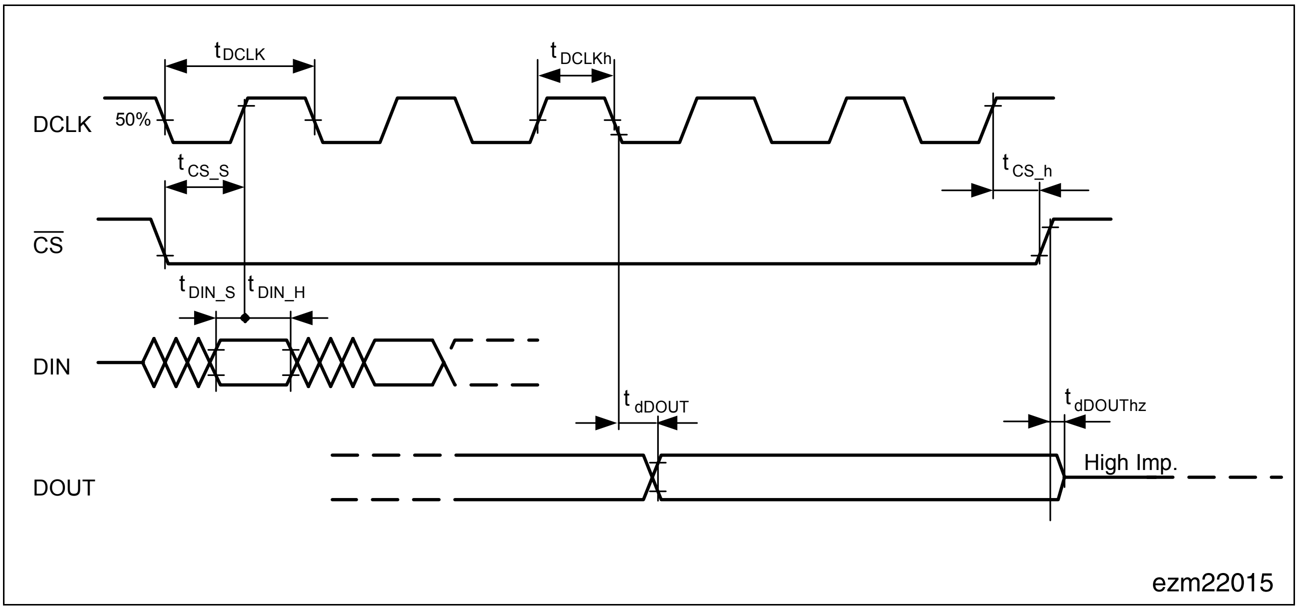


Figure 20 Microcontroller Interface Timing

Table 22 Microcontroller Interface Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of DCLK	t_{DCLK}	1/8192	–	–	ms
DCLK high time	t_{DCLKh}	–	$0.5 \times t_{DCLK}$	–	µs
CS setup time	t_{CS_s}	10	50	–	ns
CS hold time	t_{CS_h}	30	50	–	ns
DIN setup time	t_{DIN_s}	10	50	–	ns
DIN hold time	t_{DIN_h}	10	50	–	ns
DOUT delay time[1)]	t_{dDOUT}	30	–	t_{dDOUT_min} + 0.4[ns/pF] × C_{Load}[pF]	ns
DOUT delay time to high Z	$t_{dDOUThz}$	30	–	50	ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load})

6.4.5 IOM-2 Interface Timing

6.4.5.1 Single-Clocking Mode

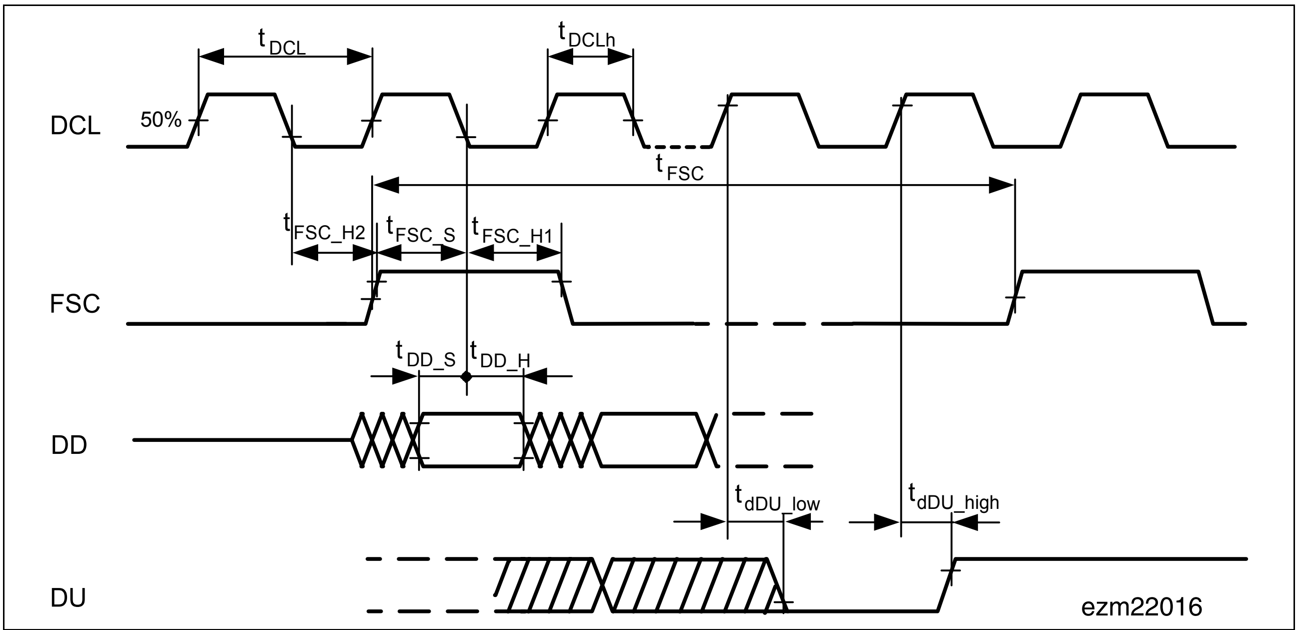


Figure 21 IOM-2 Interface Timing – Single-Clocking Mode

Table 23 IOM-2 Interface Timing – Single-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL[1]	t_{DCL}	–	1/2048	–	ms
DCL high time	t_{DCLh}	$0.4 \times t_{DCL}$	$0.5 \times t_{DCL}$	$0.6 \times t_{DCL}$	µs
Period FSC[1]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{DCL} - t_{FSC\_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DD setup time	t_{DD_s}	10	50	–	ns
DD hold time	t_{DD_h}	10	50	–	ns
DU low time[2]	t_{dDU_low}	25	–	$t_{dDU\_low\ (min)}$ + $0.4[ns/pF] \times C_{Load}[pF]$	ns
DU high time[2]	t_{dDU_high}	25	–	$t_{dDU\_high\ (min)}$ + $2 \times R_{pull\text{-}up}[k\Omega] \times C_{Load}[pF]$	ns

1) The DCL frequency must be an integer multiple of the FSC frequency.

2) DU low and high times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

6.4.5.2 Double-Clocking Mode

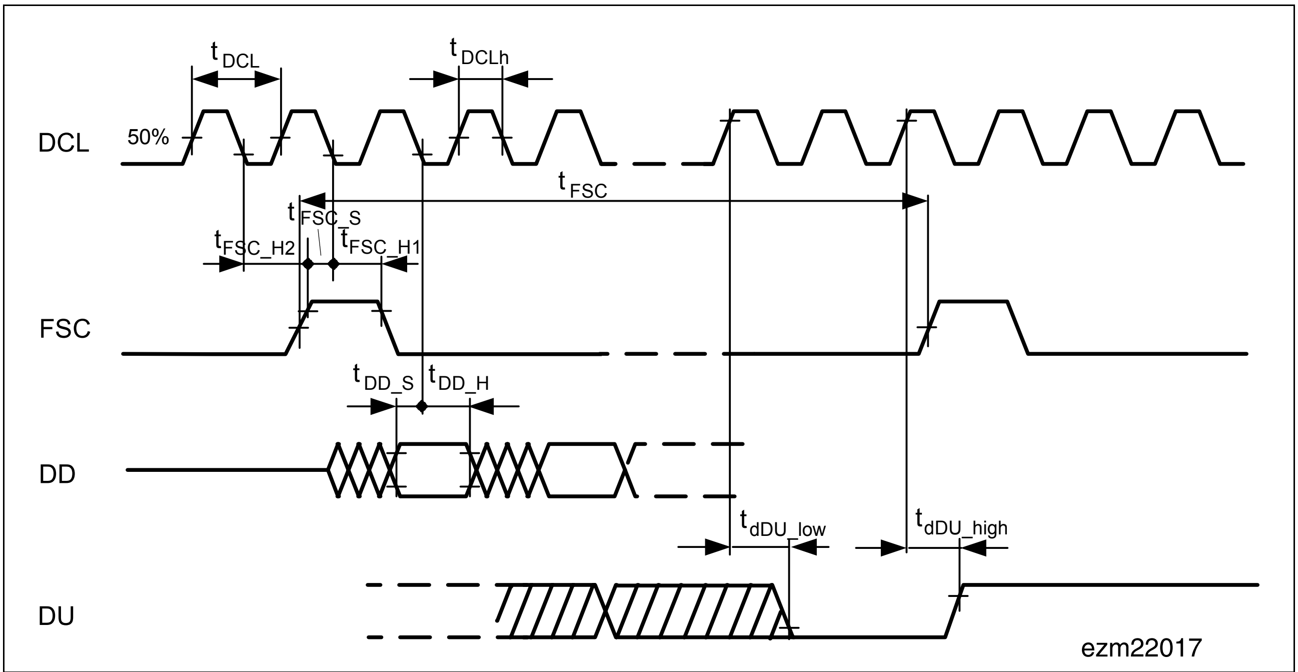


Figure 22 IOM-2 Interface Timing – Double-Clocking Mode

Table 24 IOM-2 Interface Timing – Double-Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period DCL[1)]	t_{DCL}	–	1/4096	–	ms
DCL high time	t_{DCLh}	$0.4 \times t_{DCL}$	$0.5 \times t_{DCL}$	$0.6 \times t_{DCL}$	µs
Period FSC[1)]	t_{FSC}	–	125	–	µs
FSC setup time	t_{FSC_s}	10	50	–	ns
FSC hold time 1	t_{FSC_h1}	40	50	$t_{FSC} - t_{DCL} - t_{FSC\_s}$	ns
FSC hold time 2	t_{FSC_h2}	40	50	–	ns
DD setup time	t_{DD_s}	10	50	–	ns
DD hold time	t_{DD_h}	10	50	–	ns

Table 24 IOM-2 Interface Timing – Double-Clocking Mode (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
DU low time[2)]	t_{dDU_low}	25	–	$t_{dDU\_low\ (min)}$ $+ 0.4[ns/pF] \times C_{Load}[pF]$	ns
DU high time[2)]	t_{dDU_high}	25	–	$t_{dDU\_high\ (min)} +$ $2 \times R_{pull\text{-}up}[k\Omega] \times C_{Load}[pF]$	ns

1) The DCL frequency must be an integer multiple of the FSC frequency.

2) DU low and high times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C_{Load}, R_{Pullup} > 1.5 kΩ)

7 Package Outlines

P-MQFP-64-1
(Plastic Metric Quad Flat Package)

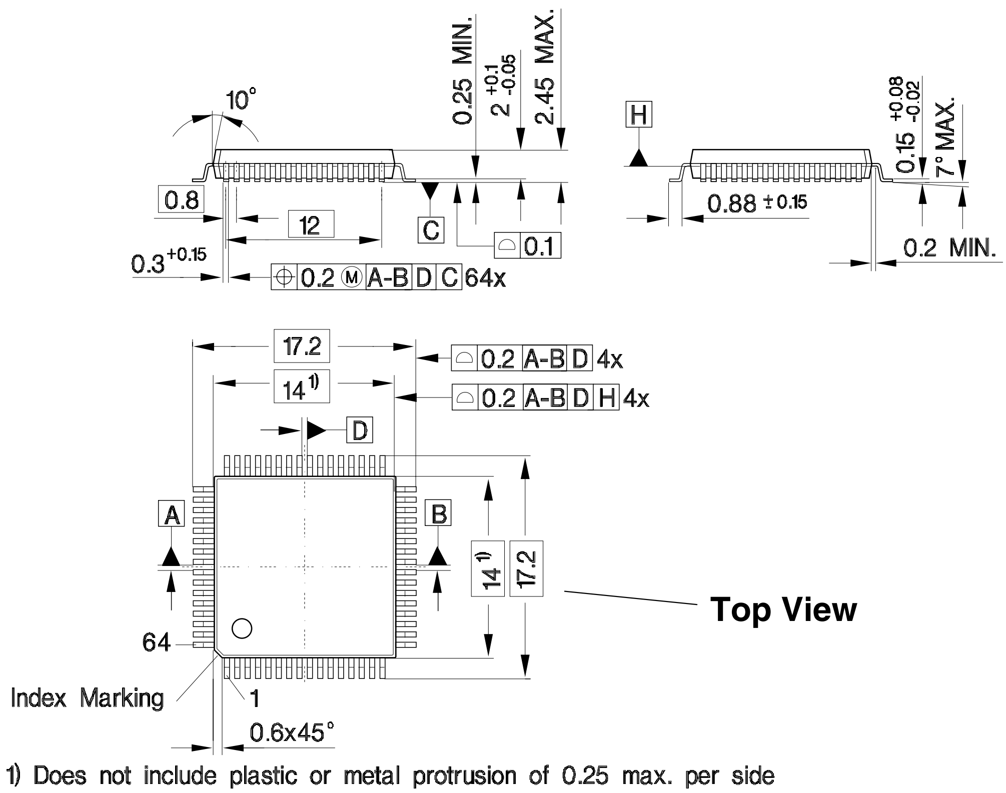


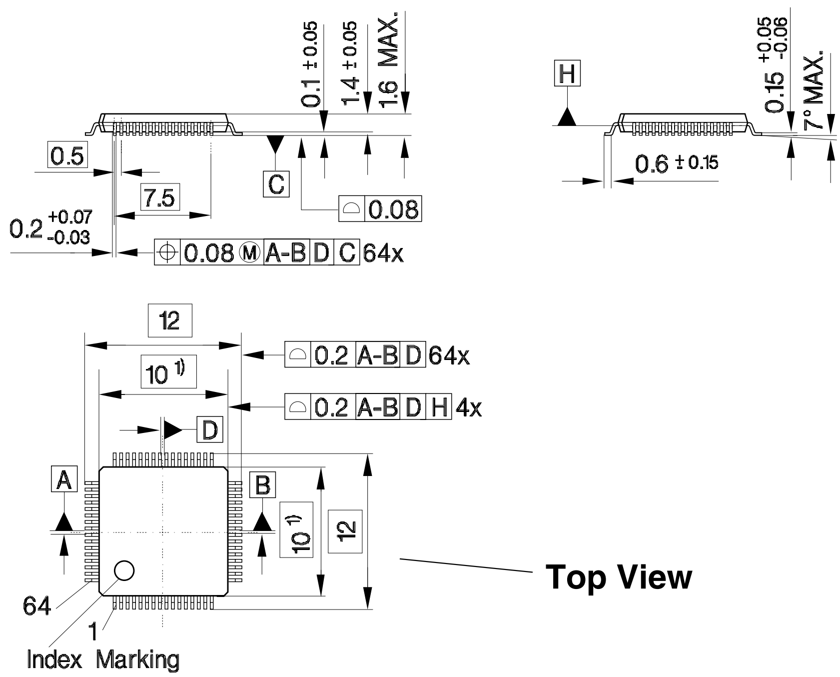
Figure 23 *SLICOFI-2x* **(PEB 3265, PEB 3264)**

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

P-TQFP-64-1
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

Gpp05613

Figure 24 ***SLICOFI-2x*** **(PEB 3265, PEB 3264)**

You can find all of our packages, sorts of packing and others in our
Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

8 Terminology

A

ACTH	Active with V_{BATH}
ACTL	Active with V_{BATL}
ACTR	Active with V_{BATR} or V_{HR} and V_{BATH}
ADC	Analog Digital Converter
AR	Attenuation Receive
AX	Attenuation Transmit
B	
BP	Band-pass
C	
CMP	Compander
Codec	Coder Decoder
COP	Coefficient Operation
CRAM	Coefficient RAM
D	
DAC	Digital Analog Converter
DSP	Digital Signal Processor
DUP	Data Upstream Persistence Counter
DuSLIC	Dual Channel Subscriber Line Interface Concept
E	
EXP	Expander
F	
FRR	Frequency Response Receive Filter
FRX	Frequency Response Transmit Filter
L	
LSSGR	Local area transport access Switching System Generic Requirements
P	
PCM	Pulse Code Modulation
PDH	Power Down High Impedance
PDRHL	Power Down Load Resistive with V_{BATH} and BGND

PDRRL	Power Down Load Resisitve with V_{BATR} and BGND
PDRH	Power Down Resistive with V_{BATH} and BGND
PDRR	Power Down Resistive with V_{BATR} and BGND
POFI	Post Filter
PREFI	Antialiasing Pre Filter
R	
RECT	Rectifier (Testloops, Levelmetering)
S	
SLIC	Subscriber Line Interface Circuit (same for all versions)
SLIC-S/-S2	Subscriber Line Interface Circuit Standard Feature Set PEB 4264/-2
SLIC-E/-E2	Subscriber Line Interface Circuit Enhanced Feature Set PEB 4265/-2
SLIC-P	Subscriber Line Interface Circuit Enhanced Power Management PEB 4266
SLICOFI-2x	Dual Channel Subscriber Line Interface Codec Filter (synonym for all versions)
SLICOFI-2	Dual Channel Subscriber Line Interface Codec Filter PEB 3265
SLICOFI-2S	Dual Channel Subscriber Line Interface Codec Filter PEB 3264
SOP	Status Operation
T	
TG	Tone Generator
TH	Transhybrid Balancing
THFIX	Transhybrid Balancing Filter (fixed)
TS	Time Slot
TSLIC-S	Twin Subscriber Line Interface Circuit Standard Feature Set PEB 3264/-2
TSLIC-E	Twin Subscriber Line Interface Circuit Standard Feature Set PEB 3265
TTX	Teletax

9 Index

http://www.infineon.com

Published by Infineon Technologies AG