

**MOTOROLA**  
**SEMICONDUCTOR**  
**TECHNICAL DATA**

Advance Information  
**TMOS ICePAK Power Module**  
**P-Channel Power MOSFET and**  
**N-Channel SENSEFET™ Product in a**  
**Full H-Bridge Configuration**

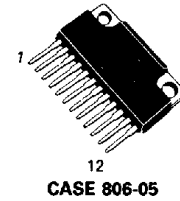
The MPM3002 is a H-Bridge power circuit with lossless current sensing capability. The upper legs of the bridge consists of P-Channel power MOSFETs and the lower legs of the bridge consist of two SENSEFET devices. This power circuit packaged in the ICePAK package is ideal for applications such as servo motor drives, stepper motor controls and switching power supplies. Features of this product include:

- P and N-Channel Power MOSFET Configuration for Ease of Drive
- Lossless Current Sensing in Each Lower Leg of the H-Bridge
- Isolated Package with 2 kV Isolation Voltage Rating
- High Power Handling Capability — 62.5 Watts
- High Peak Current Handling Capability — 25 Amperes

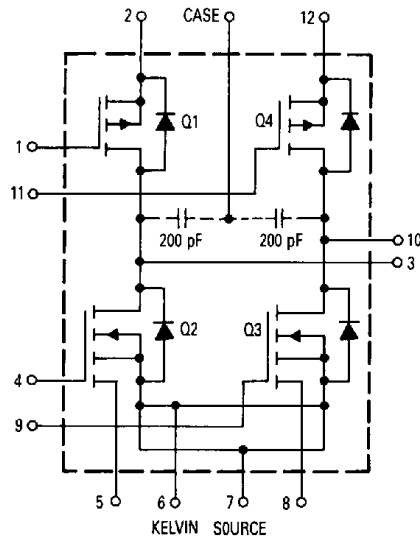
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**MPM3002**

**TMOS POWER MOSFET**  
**H-BRIDGE**  
**100 VOLTS**  
**8 AMPERES**



**MPM3002 Schematic**



This document contains information on a new product. Specifications and information herein are subject to change without notice

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage (All Types)	$V_{DSS}$	100	Volts
Drain-to-Gate Voltage ( $R_{GS} = 1M\Omega$ ) (All Types)	$V_{DGR}$	100	
Gate-to-Source Voltage (All Types)	$V_{GS}$	$\pm 20$	
Drain-to-Mirror Voltage (Q2 and Q3)	$V_{DM}$	100	
Gate-to-Mirror Voltage (Q2 and Q3)	$V_{GM}$	$\pm 20$	
Drain Current — Continuous (Q2 and Q3)	$I_D$	12	Amps
— Pulsed (Q2 and Q3)	$I_{DM}$	30	
— Continuous (Q1 and Q4)	$I_D$	8	
— Pulsed (Q1 and Q4)	$I_{DM}$	25	
— Continuous (N/P-Channel Combination)	$I_D$	8	
— Pulsed (N/P-Channel Combination)	$I_{DM}$	25	
Sense Current — Continuous (Q2 and Q3)	$I_M$	13	mA
— Pulsed (Q2 and Q3)	$I_{MM}$	33	
RMS Isolation Voltage (Any Pin to Case)	$V_{ISO}$	2000	Volts
Operating and Storage Temperature Range	$T_J, T_{stg}$	-40 to 150	$^\circ\text{C}$

**THERMAL CHARACTERISTICS**

Power Dissipation — $T_C = 25^\circ\text{C}$ (Any single device) (Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")	$P_D$	62.5 62.5 31.25	Watts
Power Derating — Derate above $T_C = 25^\circ\text{C}$ (Any single device) (Q1 and Q3 or Q1 and Q4 or Q2 and Q3 or Q2 and Q4 "On") (Q1 and Q2 and/or Q3 and Q4 "On")	$1/R_{\theta JC}$	0.5 0.5 0.25	$\text{W}/^\circ\text{C}$
Thermal Resistance — Junction to Case — Junction-to-Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2 35	$^\circ\text{C}/\text{W}$
Thermal Coupling Coefficient (Q1 to Q2 or Q4 to Q3) See Table 1 (Q1 to Q3, Q1 to Q4, Q2 to Q3 or Q2 to Q4)	$\alpha$ $\beta$	0.5 0.01	—
Maximum Lead Temperature for Soldering Purposes 1/8" from case for 5 seconds	$T_L$	260	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$ ,  $V_{MS} = 0$  unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

Drain-to-Source Breakdown Voltage (All Devices) ( $V_{GS} = 0$ , $I_D = 0.25\text{ mA}$ )	$V_{(BR)DSS}$	100	—	—	Vdc
Drain-to-Mirror Breakdown Voltage (Q2 and Q3) ( $V_{GS} = 0$ , $I_D = 0.25\text{ mA}$ )	$V_{(BR)DMS}$	100	—	—	Vdc
Zero Gate Voltage Drain Current (Any Single Device) ( $V_{DS} = 80\text{ V}$ , $V_{GS} = 0$ ) ( $V_{DS} = 80\text{ V}$ , $V_{GS} = 0$ , $T_J = 125^\circ\text{C}$ )	$I_{DSS}$	—	—	0.2 1	mAdc
Gate-Body Leakage Current — Forward (Any Single Device) ( $V_{GSF} = 20\text{ Vdc}$ , $V_{DS} = 0$ )	$I_{GSSF}$	—	—	100	nAdc
Gate Body Leakage Current — Reverse (Any Single Device) ( $V_{GSR} = 20\text{ Vdc}$ , $V_{DS} = 0$ )	$I_{GSSR}$	—	—	100	—

**ON CHARACTERISTICS\***

Gate Threshold Voltage (Any Single Device) ( $V_{DS} = V_{GS}$ , $I_D = 1\text{ mAdc}$ ) ( $T_J = 125^\circ\text{C}$ )	$V_{GS(th)}$	2 1	3 —	4.5 3.5	Vdc
Static Drain-to-Source On-Resistance (Q2 and Q3) ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 4\text{ Adc}$ )	$R_{DS(on)}$	—	—	0.15	Ohms

(continued)

**ELECTRICAL CHARACTERISTICS — continued** ( $T_J = 25^\circ\text{C}$ ,  $V_{MS} = 0$  unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
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**ON CHARACTERISTICS\***

Static Drain-to-Source On-Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 4\text{ Adc}$ )	(Q1 and Q4) $R_{DS(on)}$	—	—	0.4	Ohms
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 4\text{ Adc}$ )	(Q2 and Q3) $g_{FS}$	3	—	—	Mhos
Forward Transconductance ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 4\text{ Adc}$ )	(Q1 and Q4) $g_{FS}$	2	—	—	Mhos

**CURRENT SENSING CHARACTERISTICS** (N-Channel, Q2 and Q3)

Current Mirror Ratio (Cell Ratio) ( $R_{SENSE} = 0$ , $I_D = 8\text{ A}$ , $V_{GS} = 10\text{ V}$ )	$n$	750	—	850	—
Mirror Compliance Ratio ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 4\text{ Adc}$ )	$K_{mc}$	—	0.78	—	—
Source Active Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 4\text{ Adc}$ , $R_S = 10\text{ megohm}$ )	$r_{a(on)}$	—	140	—	m $\Omega$
Mirror Active Resistance ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 4\text{ Adc}$ )	$r_{m(on)}$	—	112	—	Ohms

**DYNAMIC CHARACTERISTICS** (All Types)

Input Capacitance	$(V_{DS} = 25\text{ V}$ , $V_{GS} = 0$ $f = 1\text{ MHz}$ )	$C_{iss}$	—	—	900	pF
Output Capacitance		$C_{oss}$	—	—	450	
Transfer Capacitance		$C_{rss}$	—	—	200	

**SWITCHING CHARACTERISTICS\*** (N-Channel, Q2 and Q3)

Turn-On Delay Time	$(V_{DD} = 25\text{ V}$ , $I_D = 4\text{ A}$ $R_{gen} = 50\text{ Ohms}$ )	$t_{d(on)}$	—	—	30	ns
Rise Time		$t_r$	—	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	—	120	
Fall Time		$t_f$	—	—	125	
Total Gate Charge	$(V_{DS} = 80\text{ V}$ , $I_D = 8\text{ A}$ $V_{GS} = 10\text{ V}$ )	$Q_g$	—	38	45	nC
Gate-Source Charge		$Q_{gs}$	—	15	—	
Gate-Drain Charge		$Q_{gd}$	—	23	—	

**SWITCHING CHARACTERISTICS\*** (P-Channel, Q1 and Q4)

Turn-On Delay Time	$(V_{DD} = 25\text{ V}$ , $I_D = 4\text{ A}$ $R_{gen} = 50\text{ Ohms}$ )	$t_{d(on)}$	—	—	25	ns
Rise Time		$t_r$	—	—	130	
Turn-Off Delay Time		$t_{d(off)}$	—	—	40	
Fall Time		$t_f$	—	—	60	
Total Gate Charge	$(V_{DS} = 80\text{ V}$ , $I_D = 8\text{ A}$ $V_{GS} = 10\text{ V}$ )	$Q_g$	—	23	30	nC
Gate-Source Charge		$Q_{gs}$	—	10	—	
Gate-Drain Charge		$Q_{gd}$	—	13	—	

**SOURCE-DRAIN DIODE CHARACTERISTICS** (N-Channel, Q2 and Q3)

Forward On-Voltage	$(I_S = 8\text{ A})$	$V_{SD}$	—	1.2	—	Vdc
Forward Turn-On Time		$t_{on}$	—	25	—	ns
Reverse Recovery Time		$t_{rr}$	—	155	—	—

**SOURCE-DRAIN DIODE CHARACTERISTICS** (P-Channel, Q1 and Q4)

Forward On-Voltage	$(I_S = 8\text{ A})$	$V_{SD}$	—	4	—	Vdc
Forward Turn-On Time		$t_{on}$	—	25	—	ns
Reverse Recovery Time		$t_{rr}$	—	150	—	—

\*Indicates Pulse Test: Pulse Width = 300  $\mu\text{s}$  Max, Duty Cycle = 2%

Note 1: Handling precautions to protect against electrostatic discharge is mandatory

Note 2: Do not use the mirror FET independent of the power FET

Note 3: It is recommended that the mirror terminal (M) be shorted to the source terminal (S) when current sensing is not required.

TYPICAL CHARACTERISTICS

N-CHANNEL

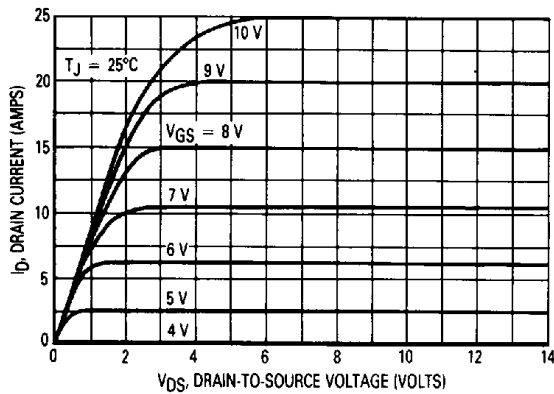


Figure 1. On-Region Characteristics

P-CHANNEL

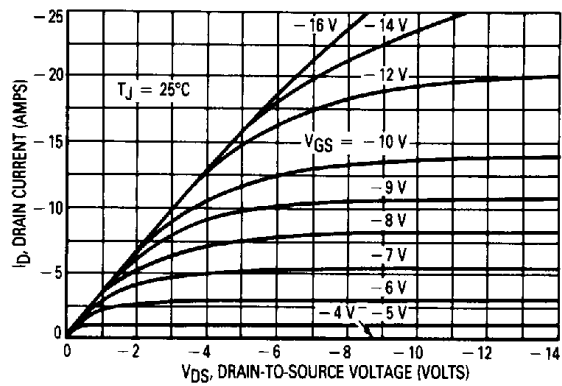


Figure 2. On-Region Characteristics

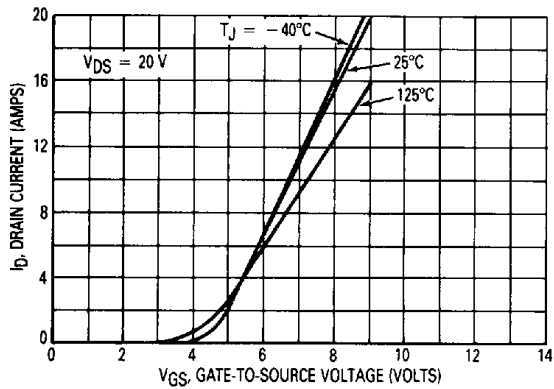


Figure 3. Transfer Characteristics

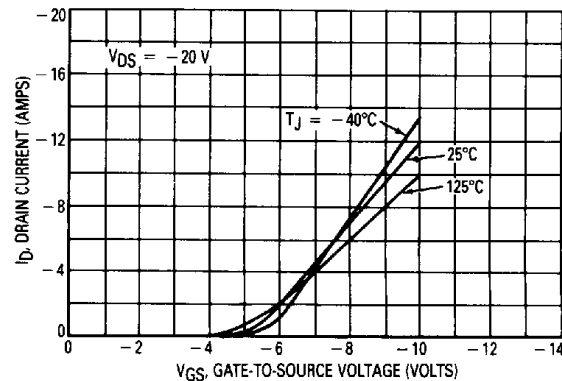


Figure 4. Transfer Characteristics

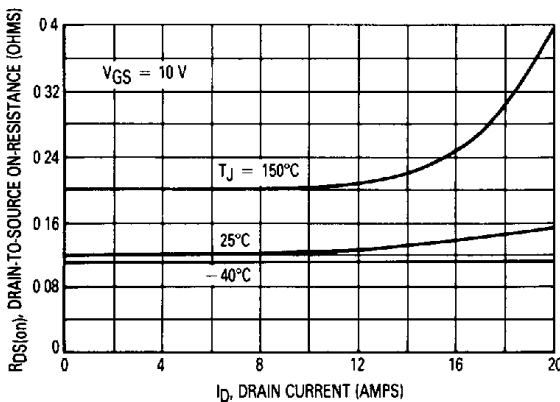


Figure 5. On-Resistance versus Drain Current

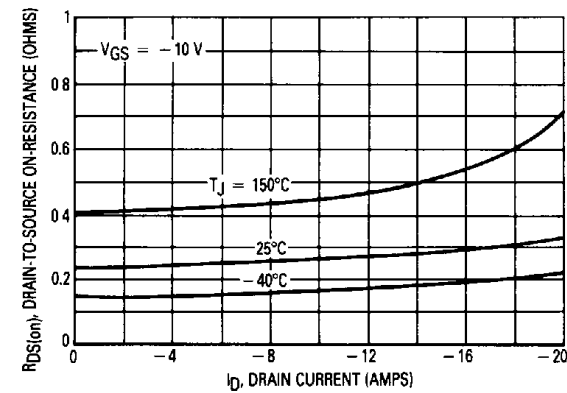


Figure 6. On-Resistance versus Drain Current

TYPICAL CHARACTERISTICS

N-CHANNEL

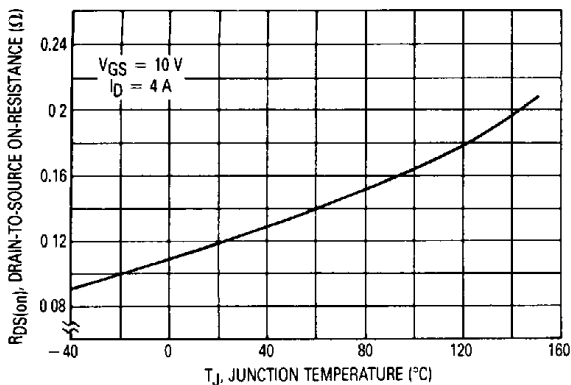


Figure 7. On-Resistance Variation with Temperature

P-CHANNEL

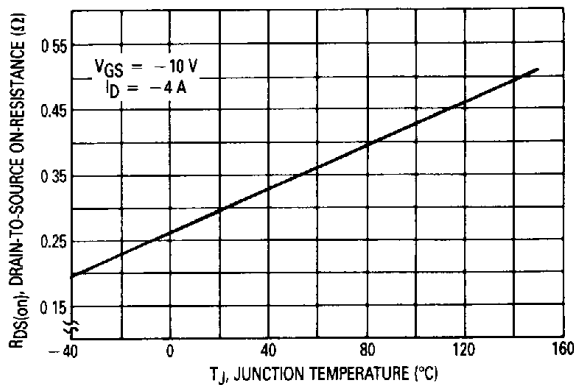


Figure 8. On-Resistance Variation with Temperature

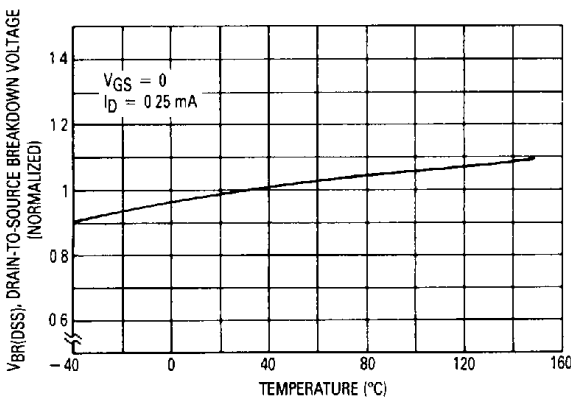


Figure 9. Drain-To-Source Breakdown Voltage Variation

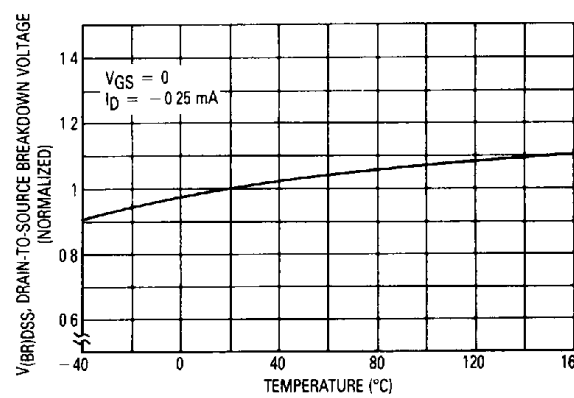


Figure 10. Drain-To-Source Breakdown Voltage Variation

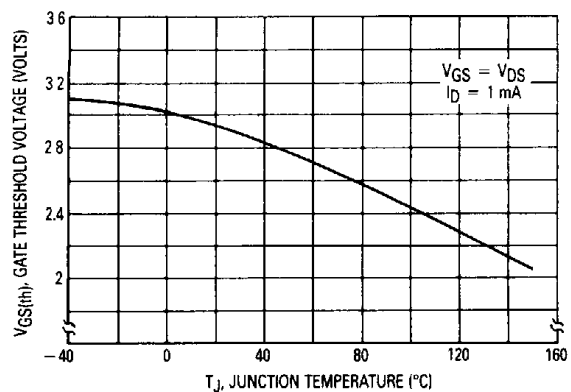


Figure 11. Gate Threshold Voltage Variation with Temperature

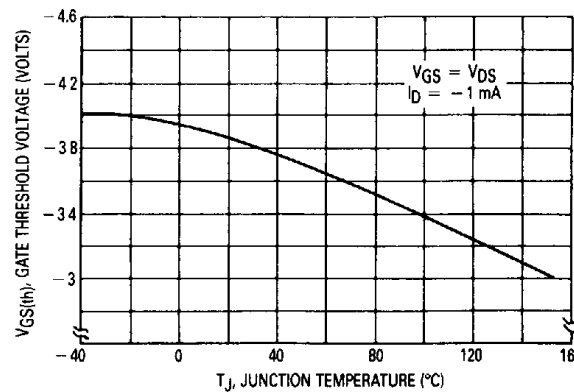


Figure 12. Gate Threshold Voltage Variation with Temperature

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TYPICAL CHARACTERISTICS

N-CHANNEL

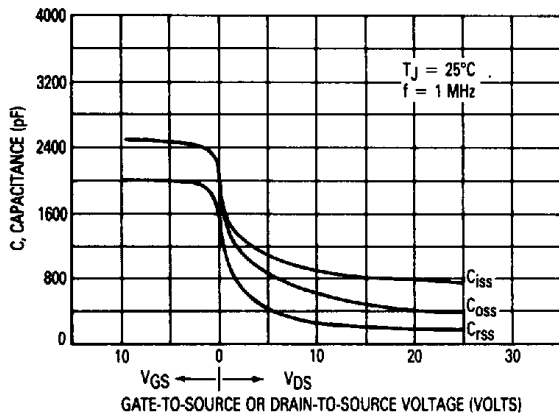


Figure 13. Capacitance Variation

P-CHANNEL

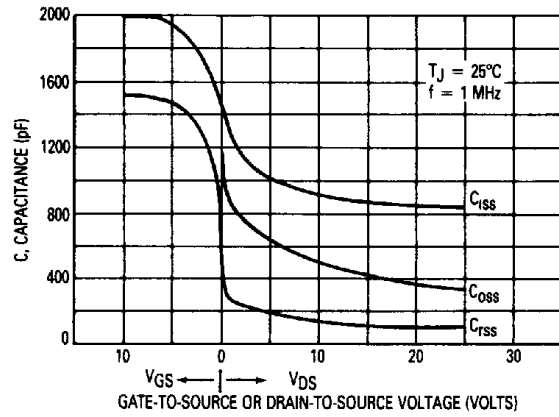


Figure 14. Capacitance Variation

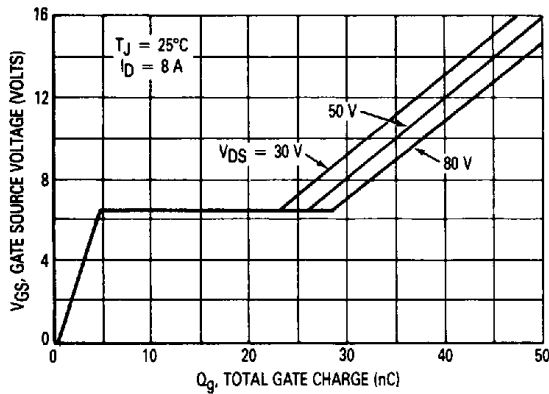


Figure 15. Stored Charge Variation

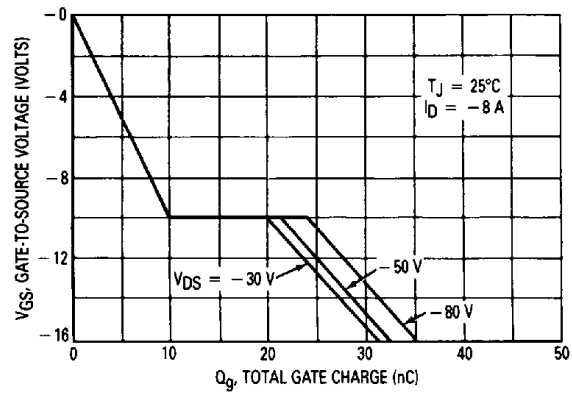


Figure 16. Stored Charge Variation

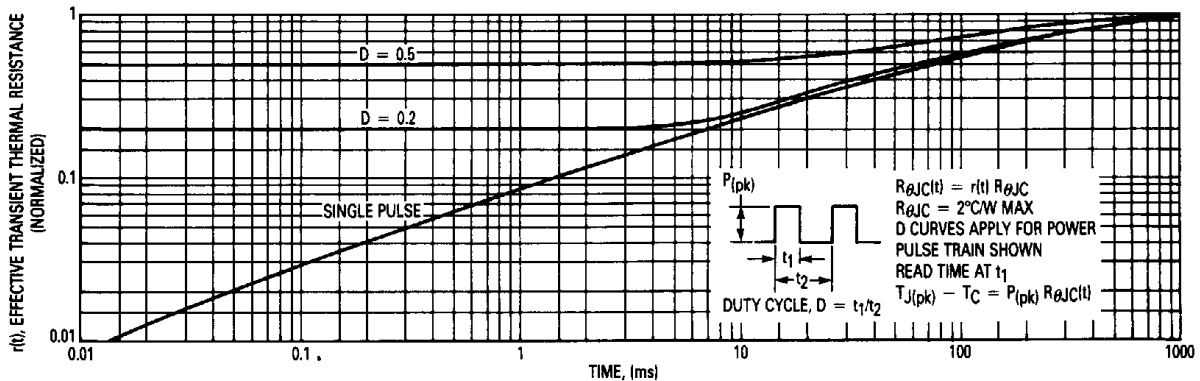


Figure 17. Thermal Response

SAFE OPERATING AREA INFORMATION

N-CHANNEL

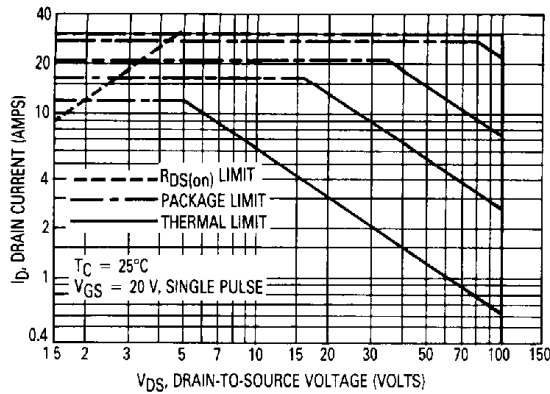


Figure 18. Maximum Rated Forward Biased Safe Operating Area

P-CHANNEL

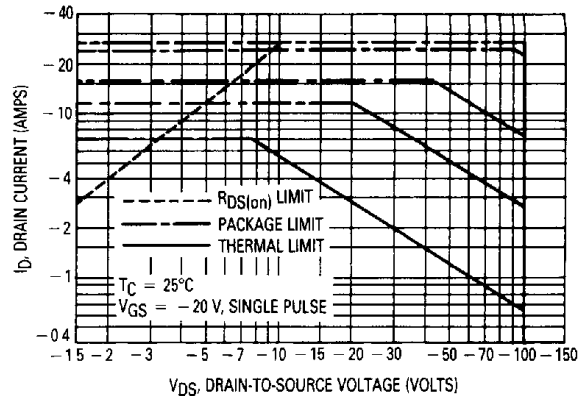


Figure 19. Maximum Rated Forward Biased Safe Operating Area

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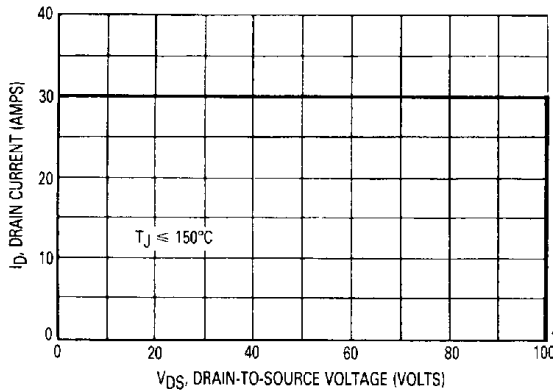


Figure 20. Maximum Rated Switching Safe Operating Area

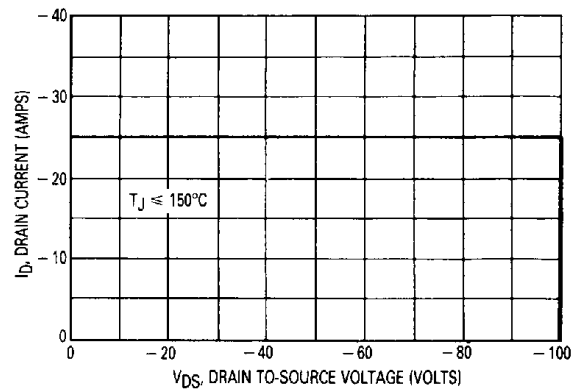


Figure 21. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

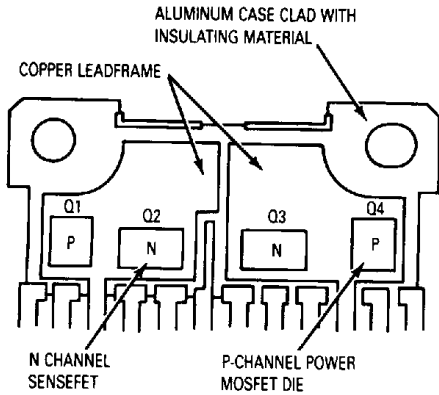
The switching safe operating area (SOA) of Figures 20 and 21 are the boundaries that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current,  $I_{DM}$  and the breakdown voltage,  $V_{(BR)DSS}$ . The switching SOA shown are applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

**THERMAL CONSIDERATIONS OF THE MPM3002**

The MPM3002 consists of two n-channel and p-channel pairs die bonded to two separate copper leadframes. An insulating material isolates the leadframes from the aluminum case. The internal construction is shown in Figure 22 below.



**Figure 22. Internal Construction of the MPM3002**

From this configuration, the simple thermal model shown in Figure 22 can be derived. Equation 3 is derived from this model.  $\alpha$  is defined as the coupling coefficient between adjacent die on a common leadframe and  $\beta$  is defined as the coupling coefficient between die on separate leadframes.

**EQUATION 3.**

$$T_{Ji} = T_C + P_{Di} R_{\theta JC} + \sum_{k=1}^4 \alpha_{ik} P_{Dk} R_{\theta JC} + \sum_{k=1}^4 \beta_{ik} P_{Dk} R_{\theta JC}$$

$\alpha$  and  $\beta$  values for different die combinations are listed in the maximum ratings. As an example of how the equa-

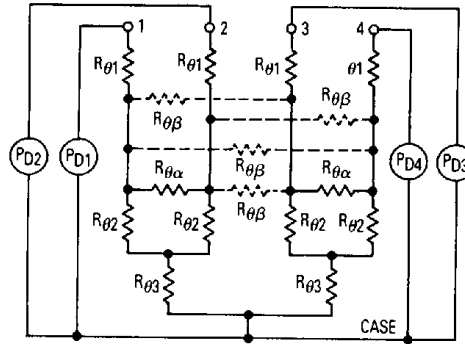
tion is used, assume that devices Q1 and Q3 are dissipating 10 watts each at a case temperature of 25°C, then calculate the junction temperature of Q1 and Q4.

FROM EQUATION 3,

$$T_{J1} = T_C + P_{D1} R_{\theta JC} + \beta_{13} P_{D3} R_{\theta JC} = 25 + (10)(2) + (0.01)(10)(2) = 47^\circ\text{C}$$

and

$$T_{J4} = T_C + \alpha_{43} P_{D3} R_{\theta JC} + \beta_{41} P_{D1} R_{\theta JC} = 25 + (0.5)(10)(2) + (0.01)(10)(2) = 37^\circ\text{C}$$



**Figure 23. Thermal Model of the MPM3002**

- $R_{\theta 1}$  = junction to leadframe thermal resistance
- $R_{\theta 2}$  = leadframe to isolator thermal resistance
- $R_{\theta 3}$  = isolator to case thermal resistance
- $R_{\theta \alpha}$  = coupling thermal resistance between adjacent die on common leadframe
- $R_{\theta \beta}$  = coupling thermal resistance between die on separate leadframes
- $R_{\theta JC} = R_{\theta 1} + R_{\theta 2} + R_{\theta 3}$

**Table 1. Thermal Coupling Coefficients**

$\alpha$ = coupling coefficient between adjacent die on same leadframe
$\beta$ = coupling coefficient between die on separate leadframes
A: $\alpha$ coefficient values:
$\alpha_{11} = \alpha_{22} = \alpha_{33} = \alpha_{44} = 0$
$\alpha_{13} = \alpha_{31} = \alpha_{23} = \alpha_{32} = \alpha_{14} = \alpha_{41} = \alpha_{24} = \alpha_{42} = 0$
$\alpha_{12} = \alpha_{21} = \alpha_{34} = \alpha_{43} = 0.5$
B: $\beta$ coefficient values
$\beta_{11} = \beta_{22} = \beta_{33} = \beta_{44} = 0$
$\beta_{12} = \beta_{21} = \beta_{34} = \beta_{43} = 0$
$\beta_{13} = \beta_{31} = \beta_{23} = \beta_{32} = \beta_{14} = \beta_{41} = \beta_{24} = \beta_{42} = 0.01$



USING SENSEFET PRODUCTS

Assuming a fully switched on SENSEFET device, current sensing can be modeled with the simple resistor divider network shown in Figure 24. In this model,  $r_b$  is the bulk drain resistance,  $r_{m(on)}$  is the active mirror on-resistance,  $r_{a(on)}$  is the power section's active on-resistance and  $r_w$  is the source wire bond resistance. Using values for  $r_{a(on)}$  and  $r_{m(on)}$  from the electrical characteristics table;  $V_{SENSE}$ ,  $R_{SENSE}$ , and drain current may be calculated from the following sensing equations.

SENSING EQUATIONS:

1.  $V_{SENSE} = I_D r_{a(on)} R_{SENSE} / (R_{SENSE} + r_{m(on)})$
2.  $R_{SENSE} = V_{SENSE} r_{m(on)} / (I_D r_{a(on)} - V_{SENSE})$
3.  $I_D = V_{SENSE} (R_{SENSE} + r_{m(on)}) / r_{a(on)} R_{SENSE}$
4.  $n = I_D / I_{SENSE}$ ; where  $R_{SENSE} = 0$
5.  $r_{a(on)} = r_{m(on)} / n$

Shown in Figure 25 is the variation of sense voltage,  $V_{SENSE}$  with drain current. When designing with SENSEFET devices there are several factors to keep in mind.

They are described as follows:

- **Maximum Sense Voltage:** The maximum sense voltage that can appear at the mirror terminal is  $(r_{a(on)} / (r_{a(on)} + r_b) \times V_{DS(on)})$ . This ratio is called the mirror compliance ratio, KMC, and defines the upper boundary for sense voltage.
- **Accuracy:** Accurate current sensing is based upon the inherent matching of  $r_{m(on)}$  with the power section's active on-resistance,  $r_{a(on)}$ . When  $R_{SENSE} = 0$ , matching and current sensing accuracy are within  $\pm 3\%$ . As  $R_{SENSE}$  is increased, sensing accuracy is reduced since mirror current becomes dependent on the ratio of internal on-resistance to an external  $R_{SENSE}$ . From a practical point of view, relatively good sensing accuracy ( $\pm 10\%$ ) is maintained up to  $R_{SENSE} = r_{m(on)} / 2$ . As  $R_{SENSE}$  is increased beyond  $r_{m(on)}$ , sensing accuracy decreases rapidly.
- **Ground Loop Errors:** Lossless current sensing is a technique that looks for 100 mV signals in a loop that may

carry tens or even hundreds of amps. The potential for ground loop errors in this kind of an application is a first order design consideration. Internal wire bond resistance, contact resistance, and external wiring resistance are all significant. Therefore, it is important to reference sense voltage measurement circuitry to the Kelvin pin rather than power ground. In addition, referencing gate drive to the Kelvin pin rather than power ground will provide faster switching speeds.

- **Noise Suppression:** Switching noise is also a first order design issue. Layout, therefore, is critical. In addition, a single pole RC filter between  $R_{SENSE}$  and the current sensing circuitry's input terminals is often desirable. A 1  $\mu$ sec time constant is generally long enough to provide adequate noise suppression and short enough to provide adequate protection during overloads. An illustration is provided in Figure 26.
- **Double Pulse Suppression:** In PWM circuits it is critically important to include double pulse suppression in the control circuit topology. If the current limit loop is allowed to oscillate at its natural frequency, failure of the SENSEFET device is likely due to excessive power dissipation. By syncing current limiting to the clock with a latch, double pulse suppression architectures solve this problem, and provide effective protection from overload stress.
- **Parasitic Diode:** In addition to the power section's usual source-drain diode, there is a mirror-drain diode in the sense cells. Like the source-drain diode, the mirror-drain diode conducts during the reverse-mode operation, however, current sense characteristics are defined only in the forward-mode operation.
- **Reverse Recovery:** In bridge circuits, when a SENSEFET device's source-drain diode is commutated a voltage spike is produced at the mirror. This spike is short since it lasts only for the drain-source diode's reverse recovery time. However, its amplitude can be an order of magnitude larger than normal sense voltages and produce unwanted overcurrent trips. Blanking, filtering, or other suppression techniques may be required in some applications.

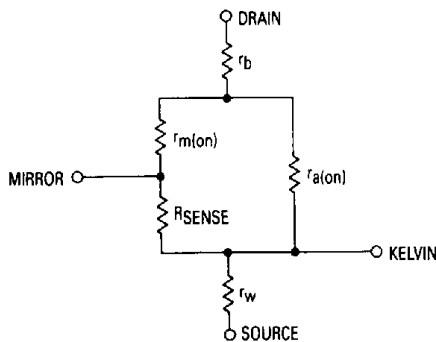


Figure 24. SENSEFET Model

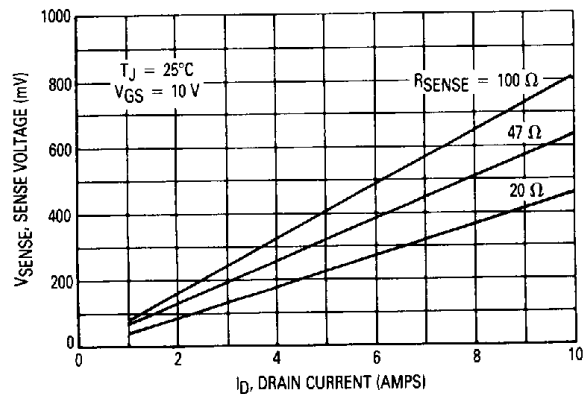


Figure 25. Sense Voltage versus Drain Current

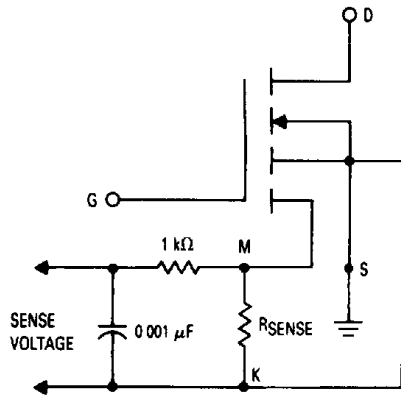


Figure 26. SENSEFET Device with Noise Suppression

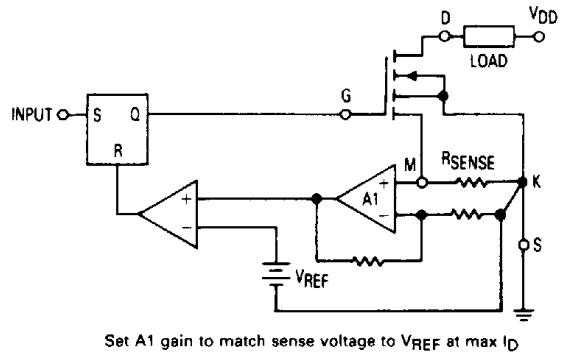


Figure 27. Typical Current Sensing with a SENSEFET Device