Voltage Controlled Oscillator

Consider MC12148 for New Designs

MC1648

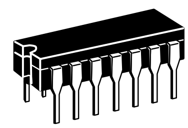
VOLTAGE CONTROLLED OSCILLATOR

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). **For Maximum Performance $Q_L \geq 100$ at Frequency of Operation.**

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase–Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2)

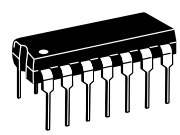
The MC1648 may be operated from a +5.0Vdc supply or a –5.2Vdc supply, depending upon system requirements.

NOTE: The MC1648 is NOT useable as a crystal oscillator.

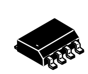


L SUFFIX
14–LEAD CERAMIC PACKAGE
CASE 632–08

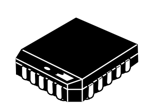
Not Recommended for New Designs



P SUFFIX
14–LEAD PLASTIC PACKAGE
CASE 646–06

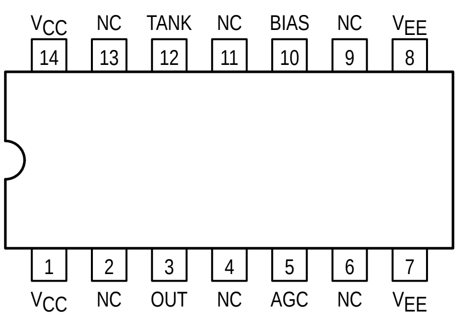


D SUFFIX
8–PIN PLASTIC SOIC PACKAGE
CASE 751–05



FN SUFFIX
20–LEAD PLCC PACKAGE
CASE 775–02

Pinout: 14–Lead Package (Top View)



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the MC1648 Non–Standard Pin Conversion Table below.

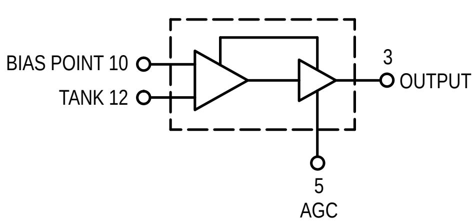
MC1648 NON–STANDARD PIN CONVERSION DATA

Package	TANK	V_{CC}	V_{CC}	OUT	AGC	V_{EE}	V_{EE}	BIAS
8 D	1	2	3	4	5	6	7	8
14 L,P	12	14	1	3	5	7	8	10
20FN	18	20	2	4	8	10	12	14

*NOTE – All unused pins are not connected.

Supply Voltage	GND Pins	Supply Pins
+5.0Vdc	7,8	1,14
–5.2Vdc	1,14	7,8

LOGIC DIAGRAM



- Input Capacitance = 6.0pF (TYP)
- Maximum Series Resistance for L (External Inductance) = 50Ω (TYP)
- Power Dissipation = 150mW (TYP)/Pkg (+5.0Vdc Supply)
- Maximum Output Frequency = 225MHz (TYP)

V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{EE} = Pin 7

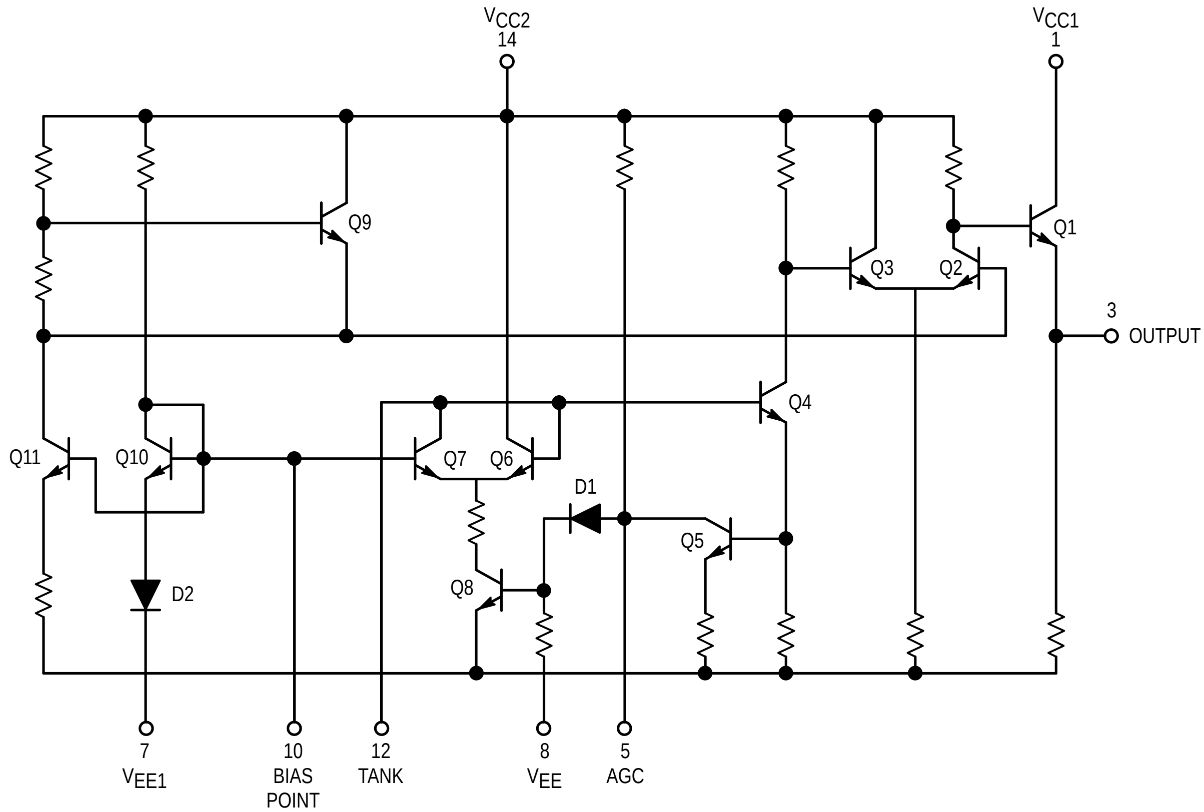


Figure 1. Circuit Schematic

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	(Volts)			mAdc
	V_{IHmax}	V_{ILmin}	V_{CC}	I_L
MC1648				
–30°C	+2.0	+1.5	+5.0	–5.0
+25°C	+1.85	+1.35	+5.0	–5.0
+85°C	+1.7	+1.2	+5.0	–5.0

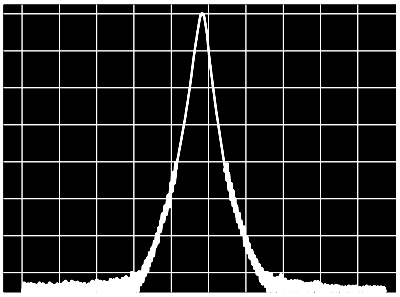
Note: SOIC "D" package guaranteed –30°C to +70°C only

ELECTRICAL CHARACTERISTICS (Supply Voltage = +5.0V)

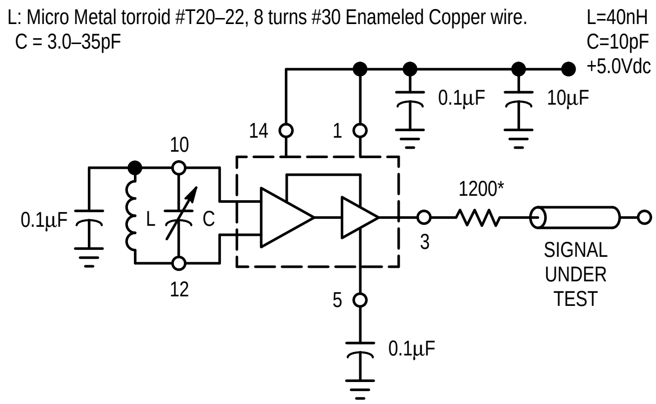
Symbol	Characteristic	–30°C		+25°C		+85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
I_E	Power Supply Drain Current	–	–	–	41	–	–	mAdc	Inputs and outputs open
V_{OH}	Logic "1" Output Voltage	3.955	4.185	4.04	4.25	4.11	4.36	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3
V_{OL}	Logic "0" Output Voltage	3.16	3.4	3.2	3.43	3.22	3.475	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3
V_{BIAS}[1]	Bias Voltage	1.6	1.9	1.45	1.75	1.3	1.6	Vdc	V_{ILmin} to Pin 12

Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
$V_{P–P}$	Peak–to–Peak Tank Voltage	–	–	–	–	400	–	–	–	–	mV	See Figure 3
Vdc	Output Duty Cycle	–	–	–	–	50	–	–	–	–	%	
f_{max}[2]	Oscillation Frequency	–	225	–	200	225	–	–	225	–	MHz	

1. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.
2. Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT–075–50 or equivalent.

Figure 2. Spectral Purity of Signal Output for 200MHz Testing

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	(Volts)			mAdc
	V_{IHmax}	V_{ILmin}	V_{EE}	I_L
MC1648				
–30°C	–3.2	–3.7	–5.2	–5.0
+25°C	–3.35	–3.85	–5.2	–5.0
+85°C	–3.5	–4.0	–5.2	–5.0

Note: SOIC "D" package guaranteed –30°C to +70°C only

ELECTRICAL CHARACTERISTICS (Supply Voltage = –5.2V)

Symbol	Characteristic	–30°C Min	–30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Condition
I_E	Power Supply Drain Current	–	–	–	41	–	–	mAdc	Inputs and outputs open
V_{OH}	Logic "1" Output Voltage	–1.045	–0.815	–0.96	–0.75	–0.89	–0.64	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3
V_{OL}	Logic "0" Output Voltage	–1.89	–1.65	–1.85	–1.62	–1.83	–1.575	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3
V_{BIAS}[1]	Bias Voltage	–3.6	–3.3	–3.75	–3.45	–3.9	–3.6	Vdc	V_{ILmin} to Pin 12

Symbol	Characteristic	–30°C Min	–30°C Typ	–30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Typ	+85°C Max	Unit	Condition
$V_{P–P}$	Peak–to–Peak Tank Voltage	–	–	–	–	400	–	–	–	–	mV	See Figure 3
Vdc	Output Duty Cycle	–	–	–	–	50	–	–	–	–	%	
f_{max}[2]	Oscillation Frequency	–	225	–	200	225	–	–	225	–	MHz	

1. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.
2. Frequency variation over temperature is a direct function of the ∆C/∆ Temperature and ∆L/∆ Temperature.

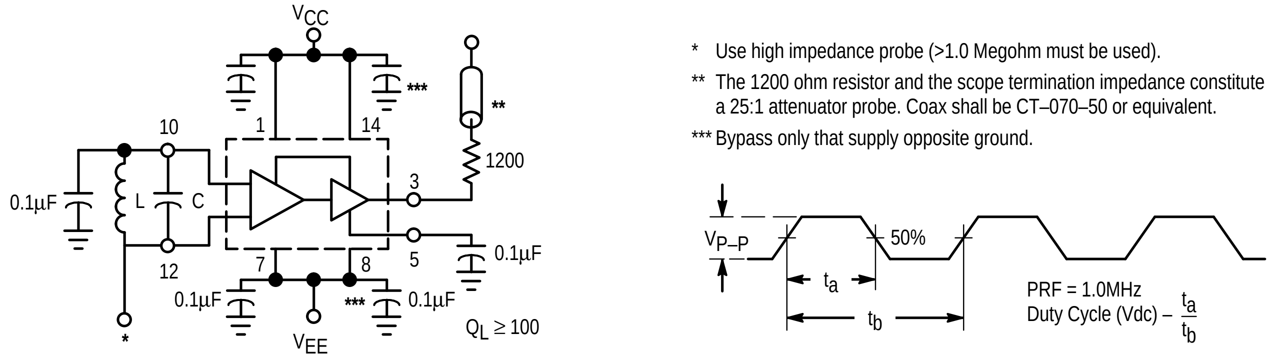


Figure 3. Test Circuit and Waveforms

OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter–coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least “2” V_{BE} above V_{EE} (≈1.4V for positive supply operation).

When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

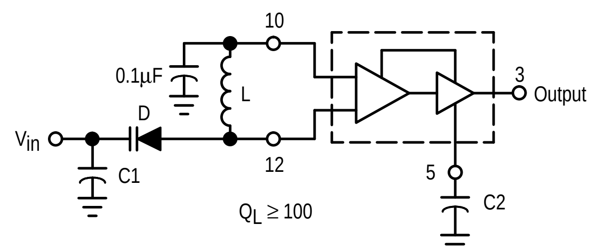
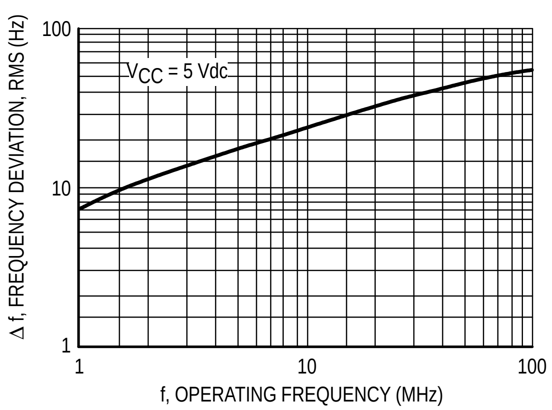
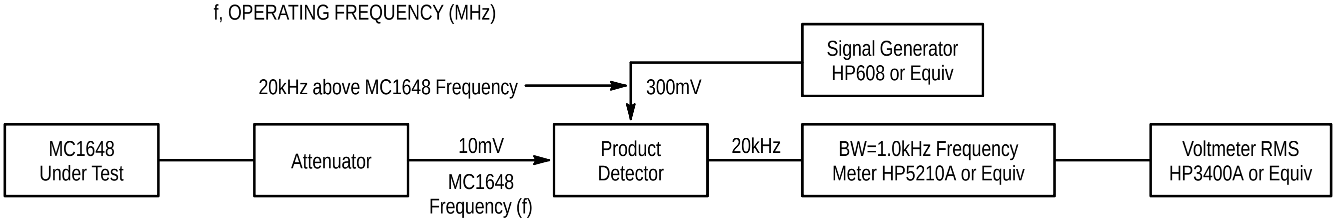


Figure 4. The MC1648 Operating in the Voltage Controlled Mode



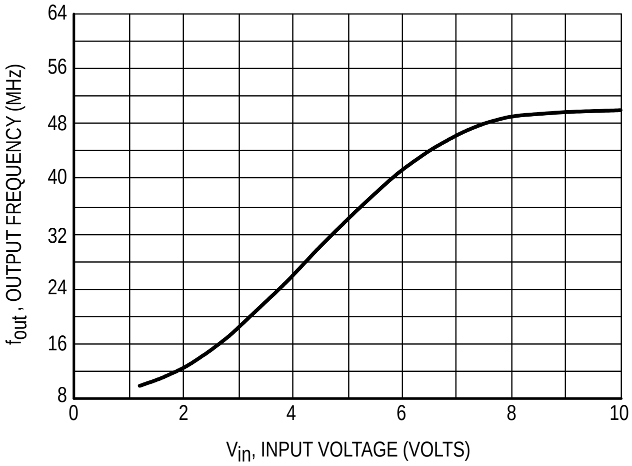
Oscillator Tank Components (Circuit of Figure 4)

f MHz	D	L µH
1.0–10	MV2115	100
10–60	MV2115	2.3
60–100	MV2106	0.15

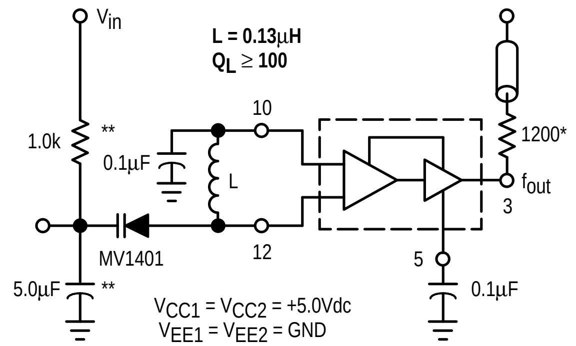


$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0Volt}}$$

Figure 5. Noise Deviation Test Circuit and Waveform



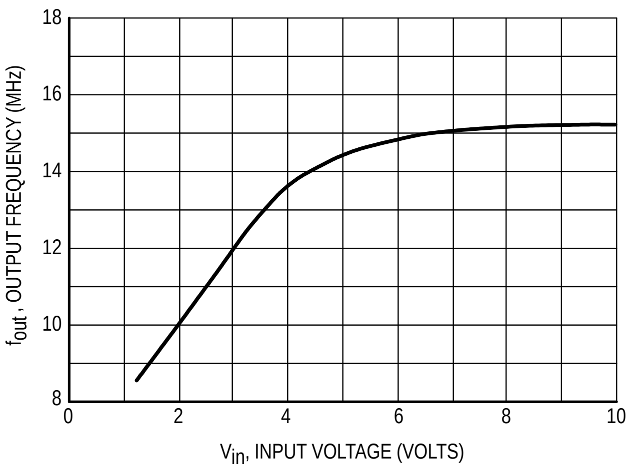
L: Micro Metal Toroidal Core #T44–10, 4 turns of No. 22 copper wire.



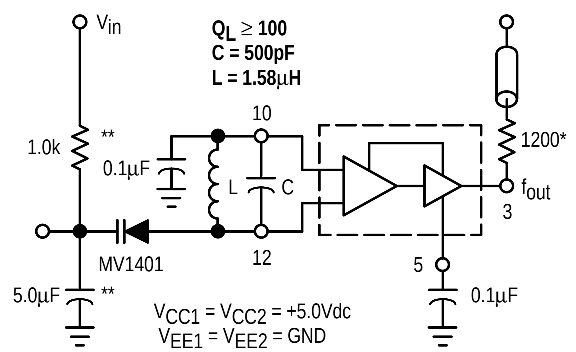
* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT–070–50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

Figure 6



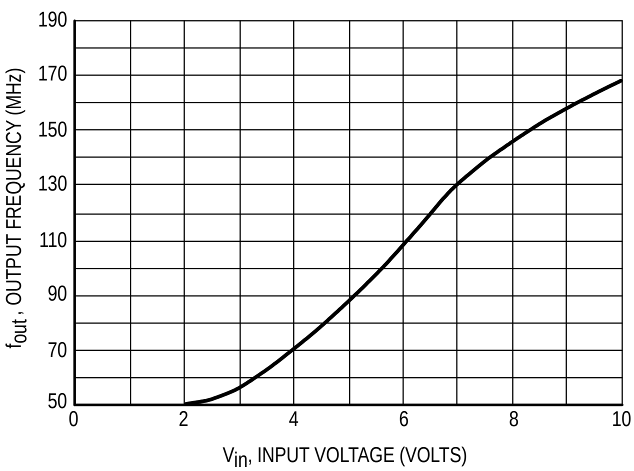
L: Micro Metal Toroidal Core #T44–10, 20 turns of No. 22 copper wire.



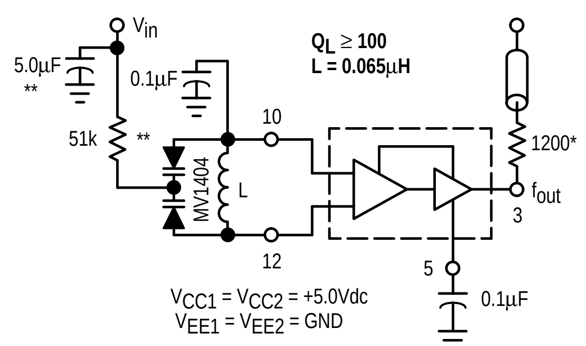
* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT–070–50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

Figure 7



L: Micro Metal Toroidal Core #T30–12, 6 turns of No. 22 copper wire.



* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT–070–50 or equivalent. NOT used in normal operation.

** Input resistor and cap are for test only. They are NOT necessary for normal operation.

Figure 8

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figure 6, Figure 7 and Figure 8. Figure 6 and Figure 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6.0pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1.0kΩ resistor in Figure 6 and Figure 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger–valued resistor (51kΩ) in Figure 8 is required to provide isolation for the high–impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $$f_{min} = \frac{1}{2\pi\sqrt{L(C_D(max) + C_S)}}$$

CS = shunt capacitance (input plus external capacitance)

CD = varactor capacitance as a function of bias voltage

Good RF and low–frequency bypassing is necessary on the power supply pins. (See Figure 2)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1.0MHz and 50MHz a 0.1µF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak–to–peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, –5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak–to–peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1.0kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a –5.2 volt supply is used). Figure 11 illustrates this principle.

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked–loops and digital frequency synthesizers, see Motorola Brochure BR504/D, Electronic Tuning Address Systems, (ETAS).

Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0Vdc supply. To extend the useful range of the device (maintain a square wave output above 175Mhz), a resistor is added to the AGC circuit at pin 5 (1.0 kohm minimum).

Figure 12 shows the MC1648 operating from +5.0Vdc and +9.0Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figure 13 and Figure 14 for 100MHz and 10MHz operation. The total collector load includes R in parallel with R_p of L1 and C1 at resonance. The optimum value for R at 100MHz is approximately 850 ohms.

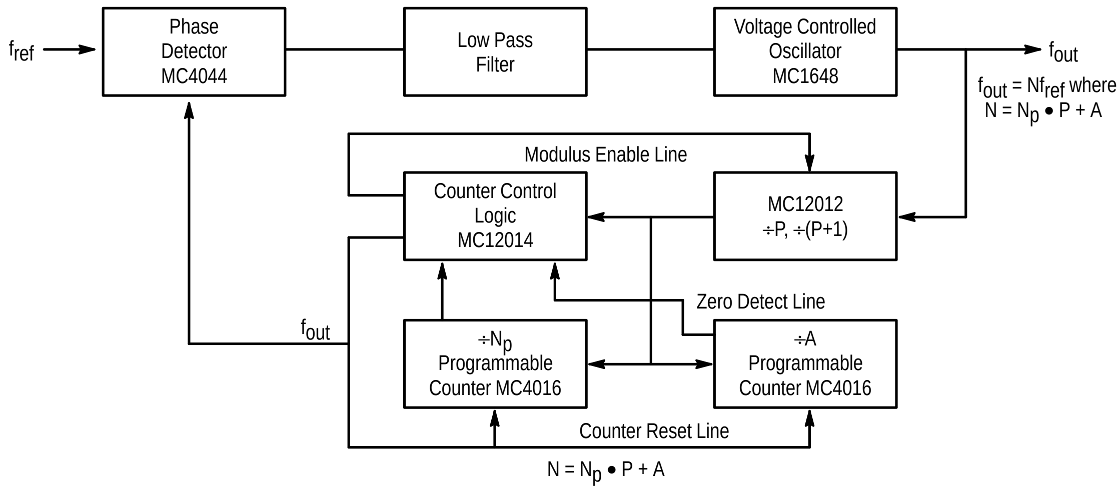


Figure 9. Typical Frequency Synthesizer Application

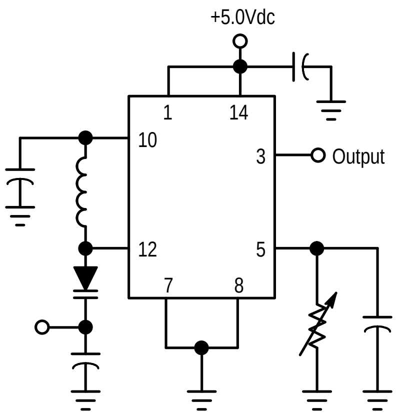


Figure 10. Method of Obtaining a Sine–Wave Output

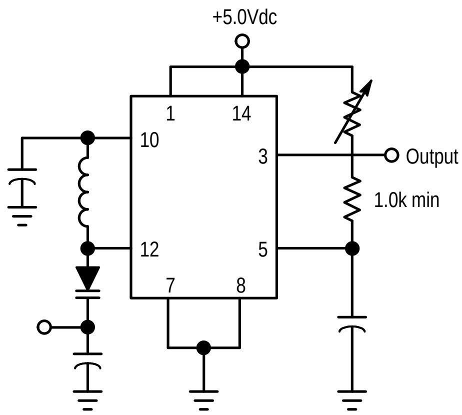


Figure 11. Method of Extending the Useful Range of the MC1648 (Square Wave Output)

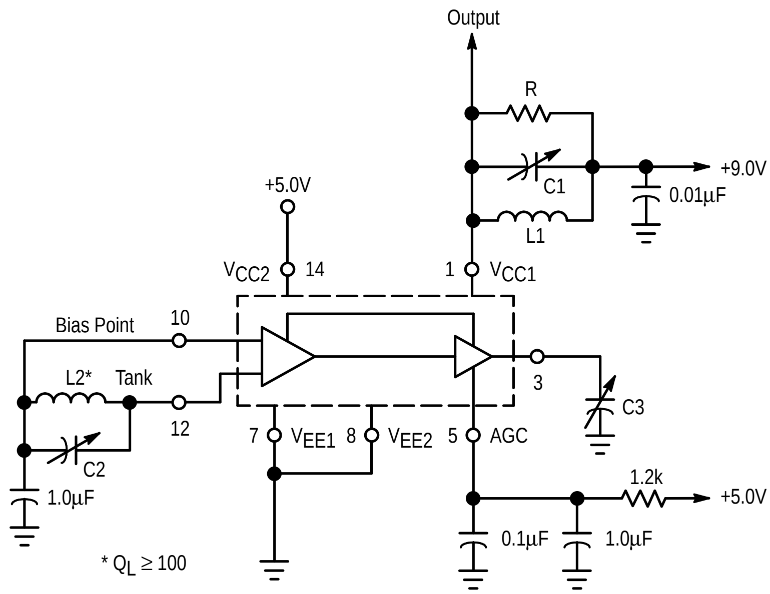
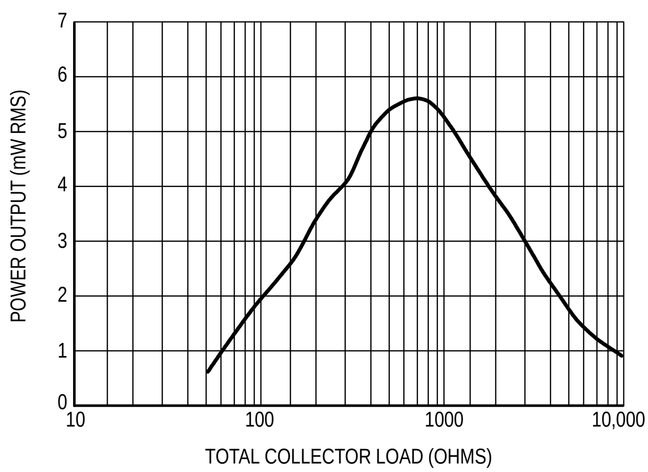
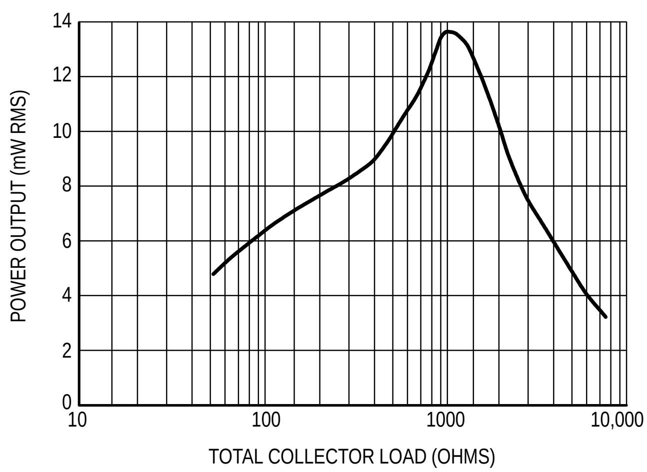


Figure 12. Circuit Used for Collector Output Operation



See test circuit, Figure 12, f = 100MHz
C3 = 3.0–35pF
Collector Tank
L1 = 0.22µH C1 = 1.0–7.0pF
R = 50Ω–10kΩ
R_P of L1 and C1 = 11kΩ @ 100MHz Resonance
Oscillator Tank
L2 = 4 turns #20 AWG 3/16” ID
C2 = 1.0–7.0pF

Figure 13. Power Output versus Collector Load

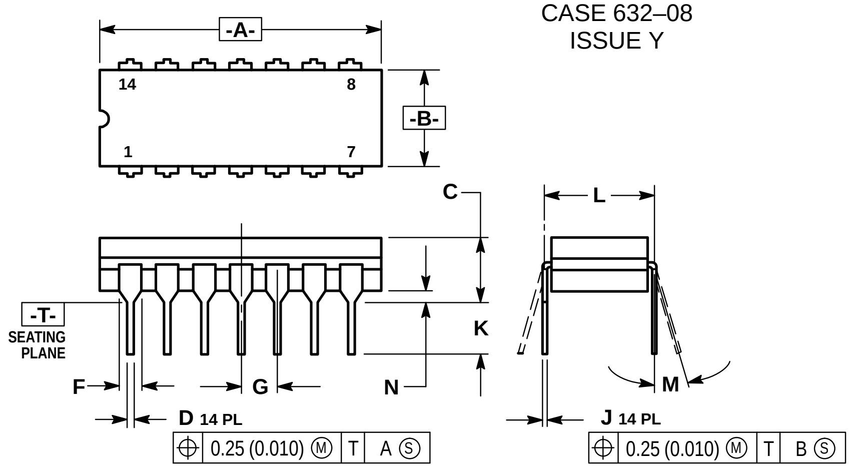


See test circuit, Figure 12, f = 10MHz
C3 = 470pF
Collector Tank
L1 = 2.7µH C1 = 24–200pF
R = 50Ω–10kΩ
R_P of L1 and C1 = 6.8kΩ @ 10MHz Resonance
Oscillator Tank
L2 = 2.7µH
C2 = 16–150pF

Figure 14. Power Output versus Collector Load

OUTLINE DIMENSIONS

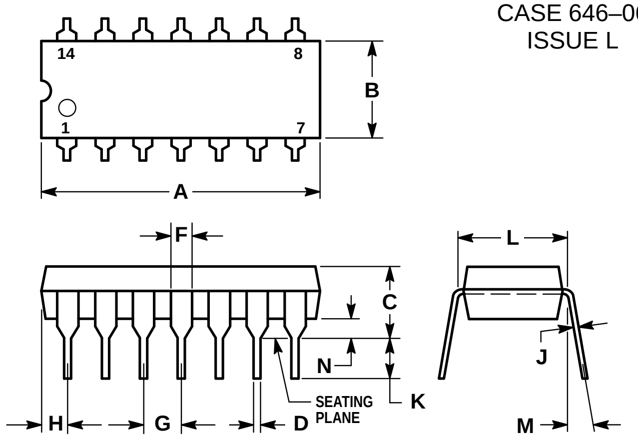
L SUFFIX
CERAMIC PACKAGE
CASE 632–08
ISSUE Y



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMESNION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

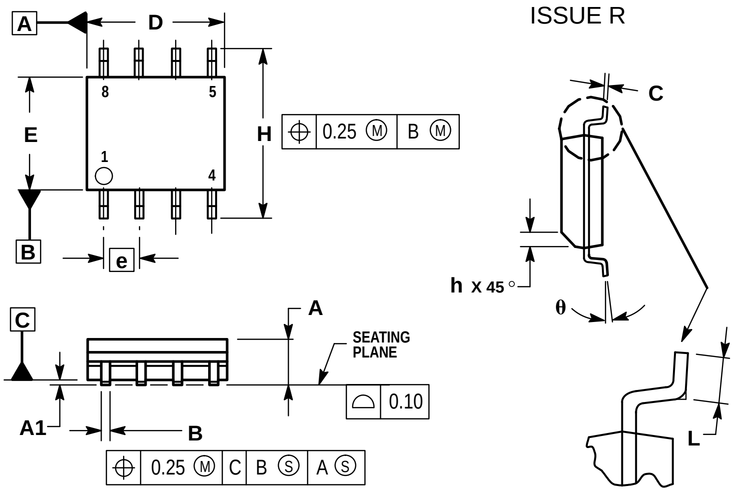
P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751–05
ISSUE R

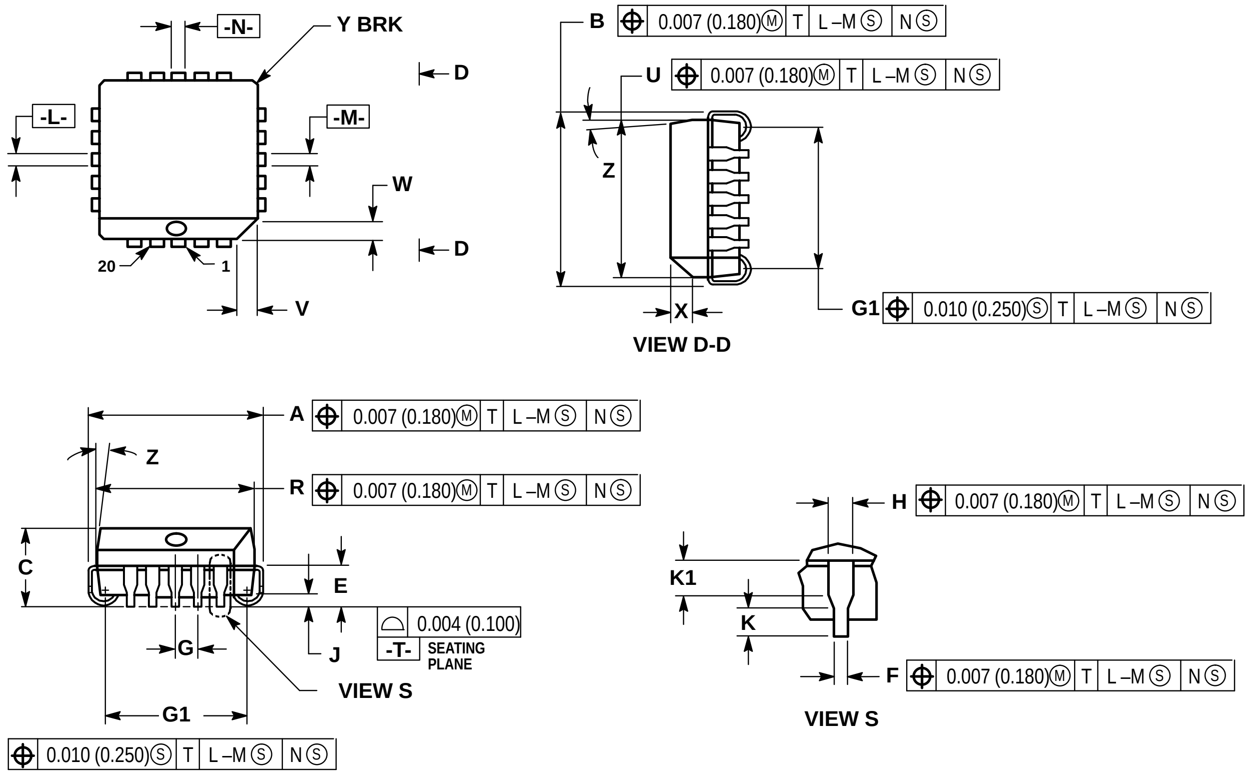


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

OUTLINE DIMENSIONS

FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 775–02
ISSUE C



NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

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