MC14067B
MC14097B

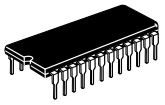
Analog Multiplexers/Demultiplexers

The MC14067 and MC14097 multiplexers/demultiplexers are digitally controlled analog switches featuring low ON resistance and very low leakage current. These devices can be used in either digital or analog applications.

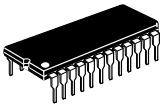
The MC14067 is a 16–channel multiplexer/demultiplexer with an inhibit and four binary control inputs A, B, C, and D. These control inputs select 1–of–16 channels by turning ON the appropriate analog switch (see MC14067 truth table.)

The MC14097 is a differential 8–channel multiplexer/demultiplexer with an inhibit and three binary control inputs A, B, and C. These control inputs select 1 of 8 pairs of channels by turning ON the appropriate analog switches (see MC14097 truth table).

- Low OFF Leakage Current
- Matched Channel Resistance
- Low Quiescent Power Consumption
- Low Crosstalk Between Channels
- Wide Operating Voltage Range: 3 to 18 V
- Low Noise
- Pin for Pin Replacement for CD4067B and CD4097B



L SUFFIX
CERAMIC
CASE 623



P SUFFIX
PLASTIC
CASE 709

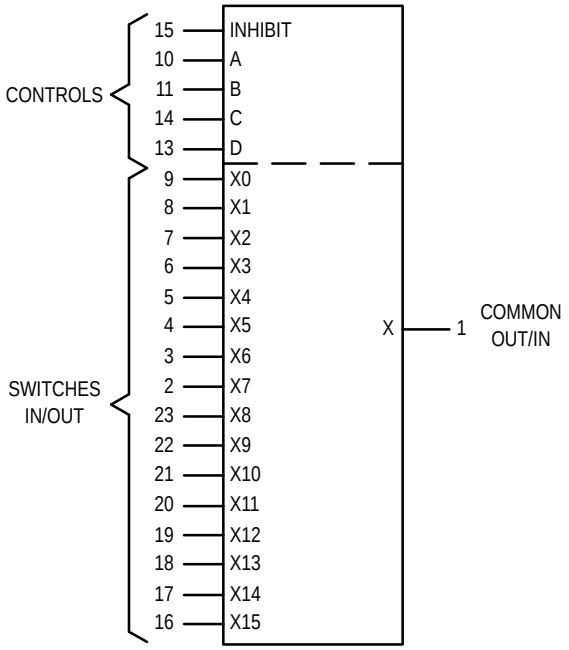
DW SUFFIX
SOIC
CASE 751E

ORDERING INFORMATION

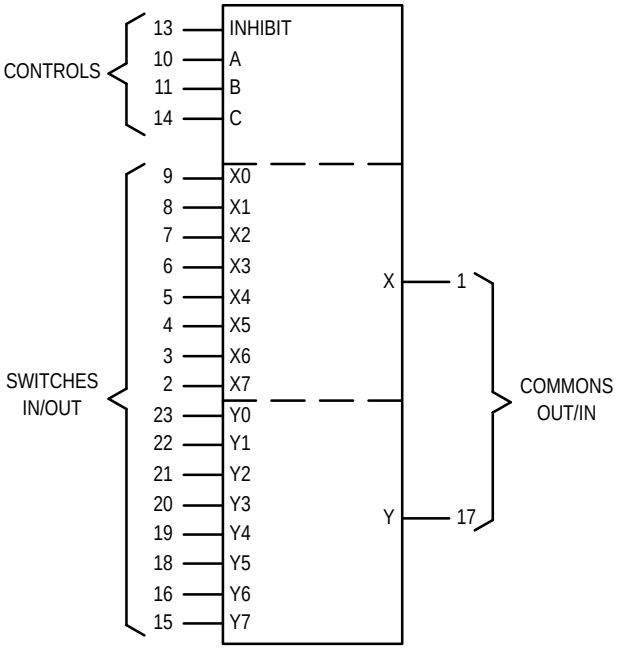
MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC

T_A = – 55° to 125°C for all packages.

MC14067B
16–Channel Analog
Multiplexer/Demultiplexer



MC14097B
Dual 8–Channel Analog
Multiplexer/Demultiplexer



REV 3
1/94

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	– 0.5 to + 18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	– 0.5 to V_{DD} + 0.5	V
I_{in}	Input Current (DC or Transient), per Control Pin	± 10	mA
I_{sw}	Switch Through Current	± 25	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	– 65 to + 150	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

* Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating:
Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic “L” Packages: – 12 mW/°C From 100°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

MC14067 TRUTH TABLE

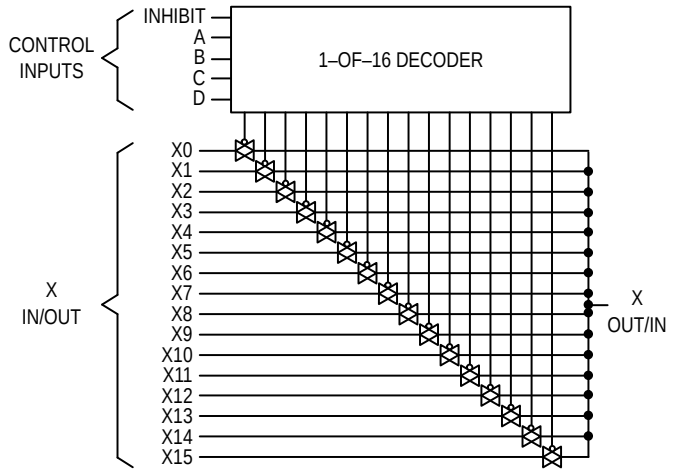
Control Inputs					Selected Channel
A	B	C	D	Inh	
X	X	X	X	1	None
0	0	0	0	0	X0
1	0	0	0	0	X1
0	1	0	0	0	X2
1	1	0	0	0	X3
0	0	1	0	0	X4
1	0	1	0	0	X5
0	1	1	0	0	X6
1	1	1	0	0	X7
0	0	0	1	0	X8
1	0	0	1	0	X9
0	1	0	1	0	X10
1	1	0	1	0	X11
0	0	1	1	0	X12
1	0	1	1	0	X13
0	1	1	1	0	X14
1	1	1	1	0	X15

MC14097 TRUTH TABLE

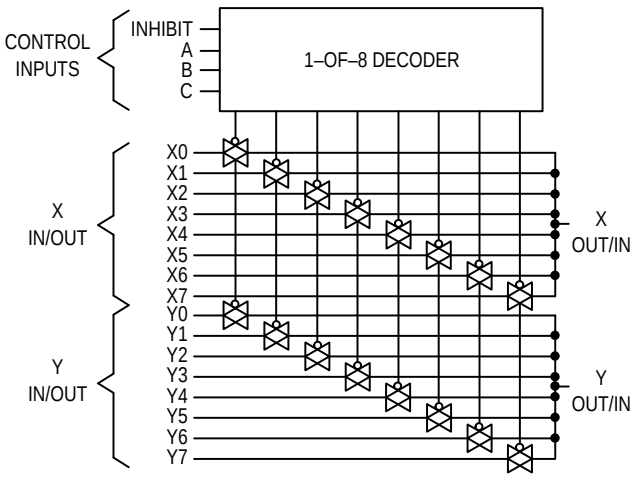
Control Inputs				Selected Channels	
A	B	C	Inh		
X	X	X	1	None	
0	0	0	0	X0	Y0
1	0	0	0	X1	Y1
0	1	0	0	X2	Y2
1	1	0	0	X3	Y3
0	0	1	0	X4	Y4
1	0	1	0	X5	Y5
0	1	1	0	X6	Y6
1	1	1	0	X7	Y7

X = Don’t Care

MC14067 FUNCTIONAL DIAGRAM



MC14097 FUNCTIONAL DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Test Conditions	– 55°C Min	– 55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
SUPPLY REQUIREMENTS (Voltages Referenced to V_{SS})											
Power Supply Voltage Range	V_{DD}	—		3.0	18	3.0	—	18	3.0	18	V
Quiescent Current Per Package	I_{DD}	5.0 10 15	Control Inputs: V_{in} = V_{SS} or V_{DD}, Switch I/O: $V_{SS} \le V_{I/O} \le V_{DD}$, and $\Delta V_{switch} \le 500$ mV**	— — —	5.0 10 20	— — —	0.005 0.010 0.015	5.0 10 20	— — —	150 300 600	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	5.0 10 15	T_A = 25°C only (The channel component, $(V_{in} - V_{out})/R_{on}$, is not included.)	Typical			(0.07 μA/kHz) f + I_{DD} (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}				μA
CONTROL INPUTS — INHIBIT, A, B, C, D (Voltages Referenced to V_{SS})											
Low–Level Input Voltage	V_{IL}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	— — —	1.5 3.0 4.0	— — —	2.25 4.50 6.75	1.5 3.0 4.0	— — —	1.5 3.0 4.0	V
High–Level Input Voltage	V_{IH}	5.0 10 15	R_{on} = per spec, I_{off} = per spec	3.5 7.0 11	— — —	3.5 7.0 11	2.75 5.50 8.25	— — —	3.5 7.0 11	— — —	V
Input Leakage Current	I_{in}	15	V_{in} = 0 or V_{DD}	—	± 0.1	—	±0.00001	± 0.1	—	1.0	μA
Input Capacitance	C_{in}	—		—	—	—	5.0	7.5	—	—	pF
SWITCHES IN/OUT AND COMMONS OUT/IN — X, Y (Voltages Referenced to V_{SS})											
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	—	Channel On or Off	0	V_{DD}	0	—	V_{DD}	0	V_{DD}	V_{p-p}
Recommended Static or Dynamic Voltage Across the Switch'* (Figure 1)	ΔV_{switch}	—	Channel On	0	600	0	—	600	0	300	mV
Output Offset Voltage	V_{OO}	—	V_{in} = 0 V, No Load	—	—	—	10	—	—	—	μV
ON Resistance	R_{on}	5.0 10 15	$\Delta V_{switch} \le 500$ mV**, $V_{in} = V_{IL}$ or V_{IH} (Control), and V_{in} 0 to V_{DD} (Switch)	— — —	800 400 220	— — —	250 120 80	1050 500 280	— — —	1300 550 320	Ω
ΔON Resistance Between Any Two Channels in the Same Package	ΔR_{on}	5.0 10 15		— — —	70 50 45	— — —	25 10 10	70 50 45	— — —	135 95 65	Ω
Off–Channel Leakage Current (Figure 2)	I_{off}	15	$V_{in} = V_{IL}$ or V_{IH} (Control) Channel to Channel or Any One Channel	—	± 100	—	± 0.05	± 100	—	±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	—	Inhibit = V_{DD}	—	—	—	10	—	—	—	pF
Capacitance, Common O/I	$C_{O/I}$	—	Inhibit = V_{DD} (MC14067B) (MC14097B)	— —	— —	— —	100 60	— —	— —	— —	pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	— —	Pins Not Adjacent Pins Adjacent	—	—	—	0.47	—	—	—	pF

Data labeled "Typ" is not to be used for design purposes, but is intended as an indication of the IC's potential performance.

** For voltage drops across the switch (ΔV_{switch}) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn; i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	$V_{DD} - V_{SS}$ Vdc	Typ #	Max	Unit
Propagation Delay Times	t_{PLH}, t_{PHL}				ns
Channel Input–to–Channel Output (R_L = 200 kΩ)					
MC14067B	(Figure 3)	5.0	35	90	
		10	15	40	
		15	12	30	
MC14097B		5.0	25	65	ns
		10	10	25	
		15	7	18	
Control Input–to–Channel Output	t_{PZH}, t_{PZL}				ns
Channel Turn–On Time (R_L = 10 kΩ)					
MC14067B/097B	(Figure 4)	5.0	240	600	
		10	115	290	
		15	75	190	
Channel Turn–Off Time (R_L = 300 kΩ)	t_{PHZ}, t_{PLZ}				ns
MC14067B/097B					
	(Figure 4)	5.0	250	625	
		10	120	300	
		15	75	190	
Any Pair of Address Inputs to Output	t_{PLH}, t_{PHL}				ns
MC14067B					
		5.0	280	700	
		10	115	290	
		15	85	215	
MC14097B					ns
	(Figure 10)	5.0	250	625	
		10	100	250	
		15	75	190	
Second Harmonic Distortion	—	10	0.3	—	%
(R_L = 10 kΩ, f = 1 kHz, V_{in} = 5 V_{p-p})					
ON Channel Bandwidth	BW				MHz
[R_L = 1 kΩ, V_{in} = 1/2 ($V_{DD} - V_{SS}$) $_{p-p}$(sine–wave)]					
20 Log10 (V_{out}/V_{in}) = – 3 dB MC14067B	(Figure 5)	10	15	—	
MC14097B		10	25	—	
Off Channel Feedthrough Attenuation	—	10	– 40	—	dB
[R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{SS}) $_{p-p}$(sine–wave)]					
f_{in} = 20 MHz – MC14067B	(Figure 5)				
f_{in} = 12 MHz – MC14097B					
Channel Separation	—	10	– 40	—	dB
[R_L = 1 kΩ, V_{in} = 1/2 (V_{DD}–V_{SS}) $_{p-p}$ (sine–wave)]					
f_{in} = 20 MHz	(Figure 6)				
Crosstalk, Control Inputs–to–Common O/I	—	10	30	—	mV
(R1 = 1 kΩ, R_L = 10 kΩ,					
Control t_r = t_f = 20 ns, Inhibit = V_{SS})	(Figure 7)				

#Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

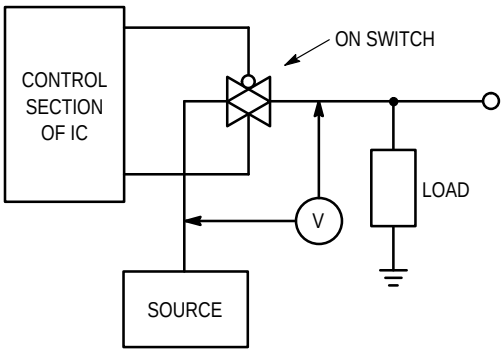


Figure 1. ΔV Across Switch

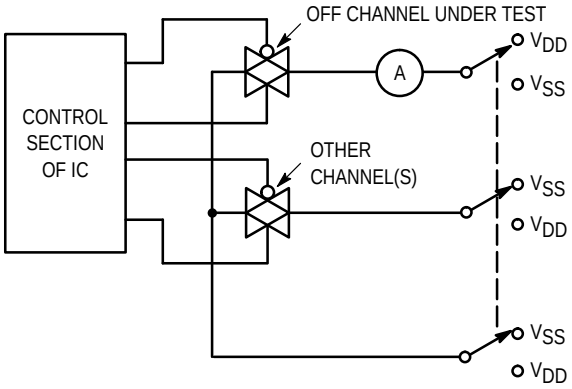
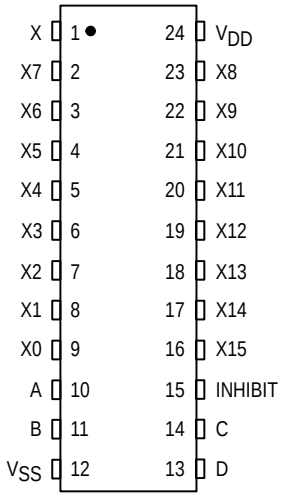
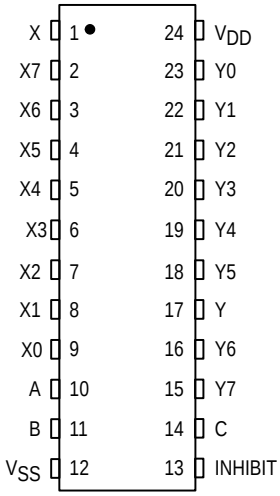


Figure 2. Off Channel Leakage

MC14067B
PIN ASSIGNMENT



MC14097B
PIN ASSIGNMENT



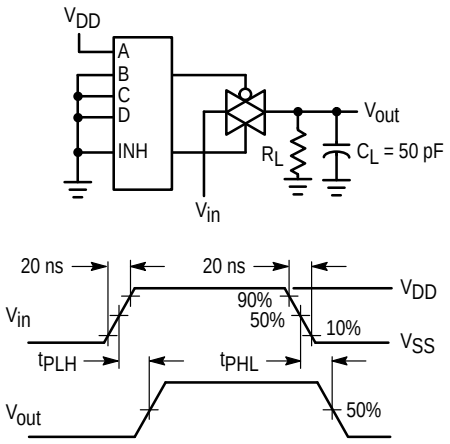


Figure 3. Propagation Delay Test Circuit and Waveforms V_{in} to V_{out}

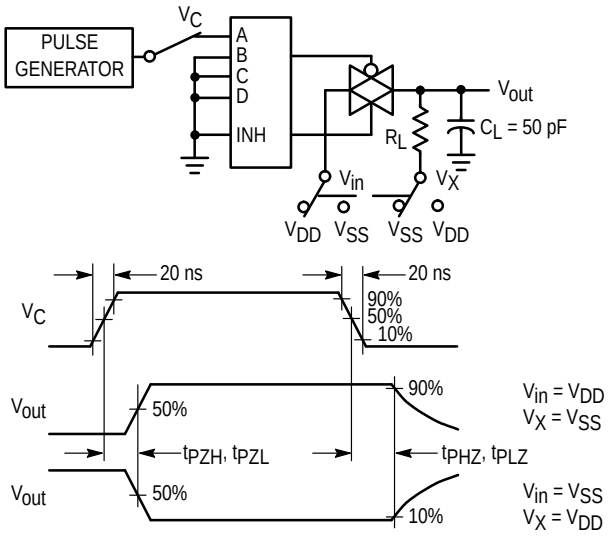


Figure 4. Turn–On and Delay Turn–Off Test Circuit and Waveforms

A, B, and C inputs used to turn ON or OFF the switch under test.

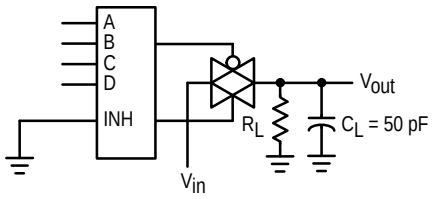


Figure 5. Bandwidth and Off–Channel Feedthrough Attenuation

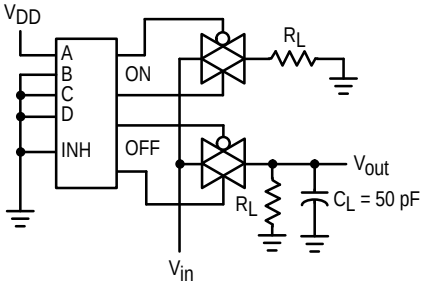


Figure 6. Channel Separation (Adjacent Channels Used for Setup)

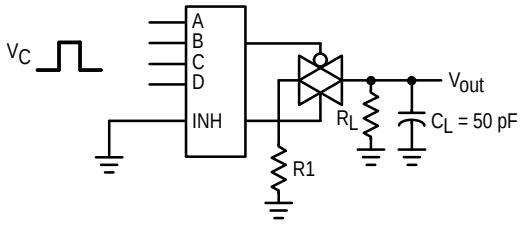


Figure 7. Crosstalk, Control to Common O/I

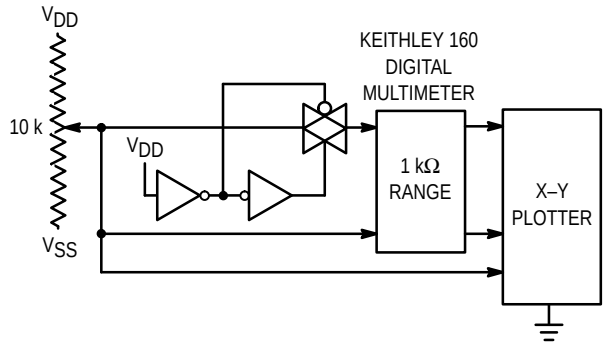


Figure 8. Channel Resistance (R_{ON}) Test Circuit

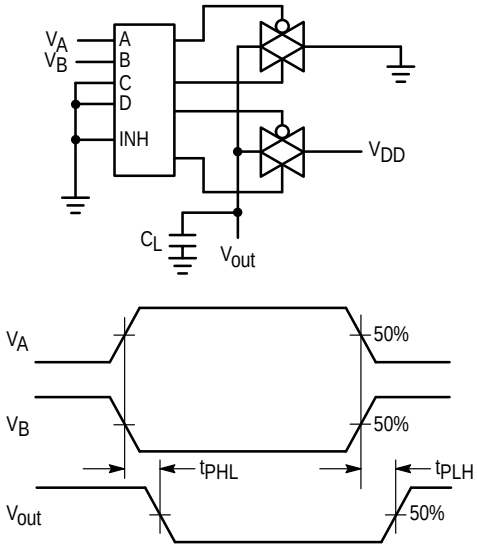


Figure 9. Propagation Delay, Any Pair of Address Inputs to Output

TYPICAL RESISTANCE CHARACTERISTICS

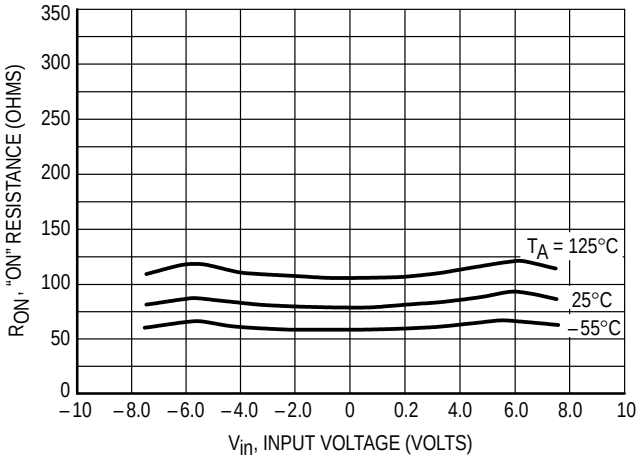


Figure 10. V_{DD} = 7.5 V, V_{SS} = – 7.5 V

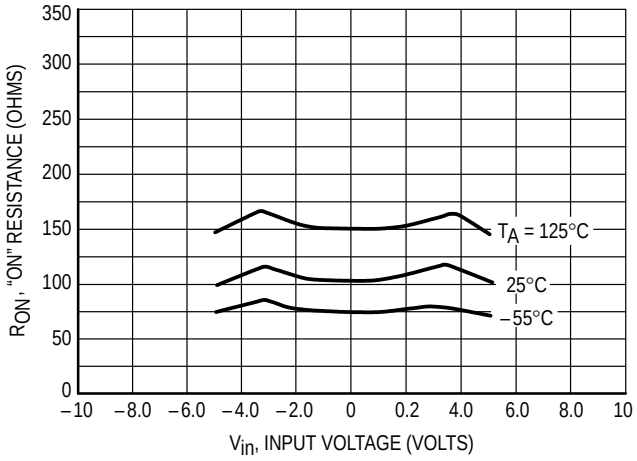


Figure 11. V_{DD} = 5.0 V, V_{SS} = – 5.0 V

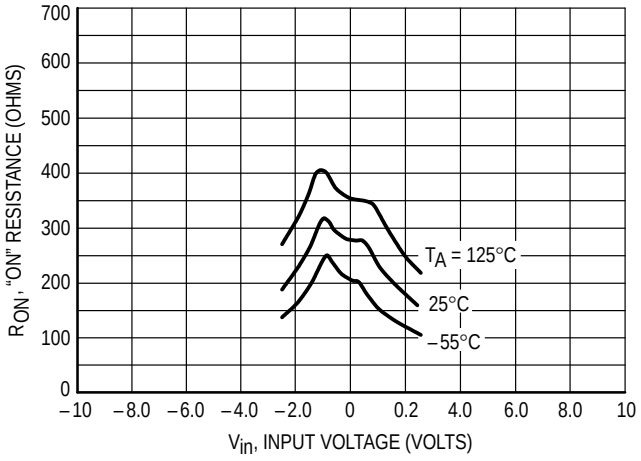


Figure 12. V_{DD} = 2.5 V, V_{SS} = – 2.5 V

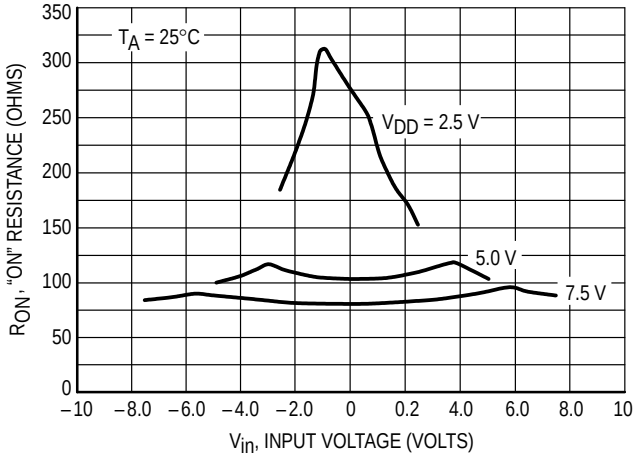


Figure 13. Comparison at 25°C, $V_{DD} = -V_{SS}$

APPLICATIONS INFORMATION

Figure A illustrates use of the Analog Multiplexer/Demultiplexer. The 0–to–5 volt Digital Control signal is used to directly control a 5 V_{p-p} analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example. V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{SS}. The analog voltage must swing neither higher than V_{DD} nor lower than V_{SS}. The example shows a 5 V_{p-p} signal which allows no margin at either peak. If voltage transients above V_{DD} and/or below V_{SS} are anticipated on the analog channels, external diodes (D_X) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The absolute maximum potential difference between V_{DD} and V_{SS} is 18.0 volts. Most parameters are specified up to 15 V which is the recommended maximum difference between V_{DD} and V_{SS}.

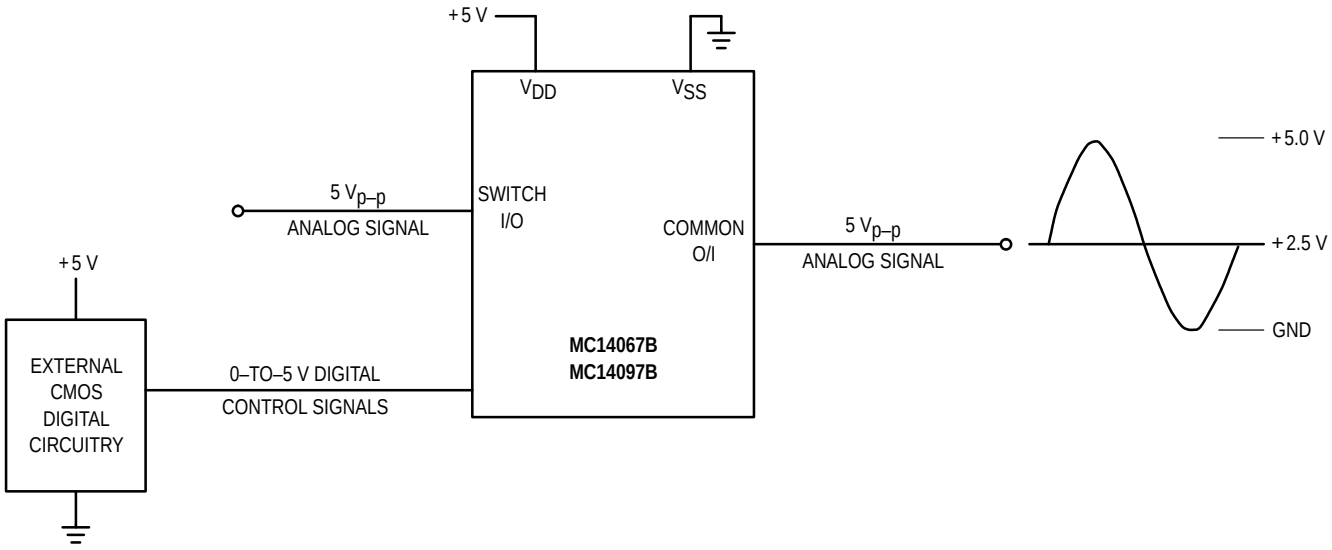


Figure A. Application Example

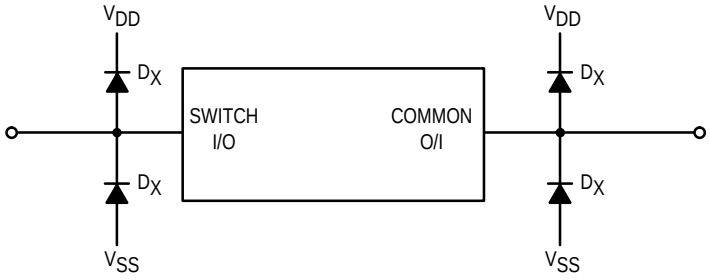
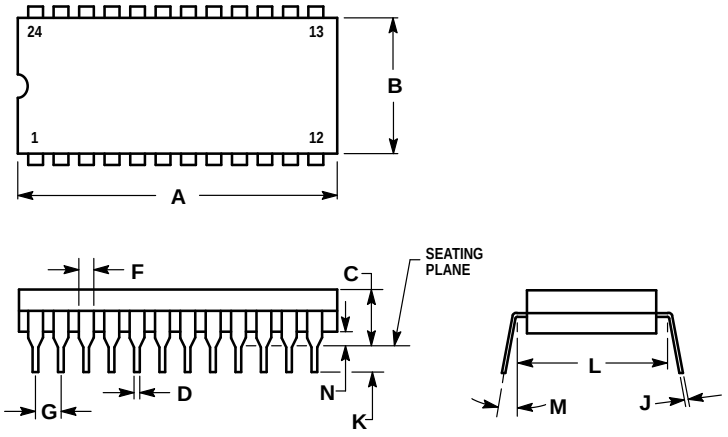


Figure B. External Germanium or Schottky Clipping Diodes

OUTLINE DIMENSIONS

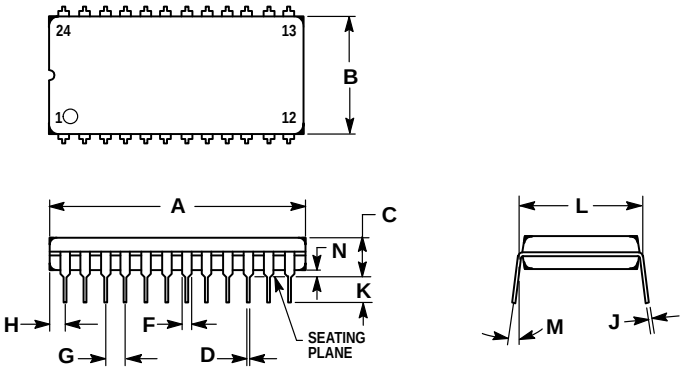
L SUFFIX
CERAMIC DIP PACKAGE
CASE 623–05
ISSUE M



NOTES:
1. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.27	0.020	0.050

P SUFFIX
PLASTIC DIP PACKAGE
CASE 709–02
ISSUE C

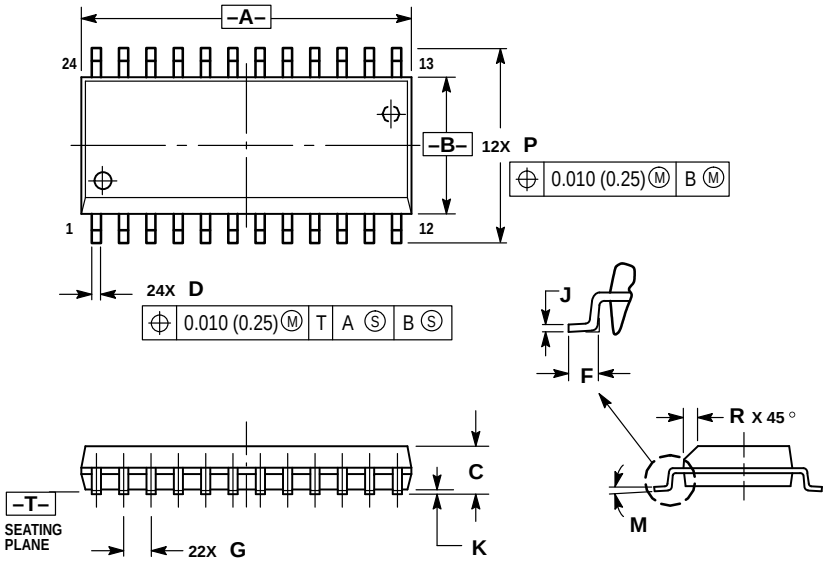


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.03	0.065	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0 °	15 °	0 °	15 °
N	0.51	1.02	0.020	0.040

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751E–04
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0 °	8 °	0 °	8 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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