

**80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER**

**DESCRIPTION**

The M50524FP, an IC which has been developed by using the silicon gate CMOS process, has two sets of built-in 40-bit liquid crystal drive circuits, and outputs display data which is transferred serially from the display controller to the liquid crystal by conversion to a liquid crystal display waveform.

In addition, each of the drive circuits can be used for either the scanning side (common) or data side (column).

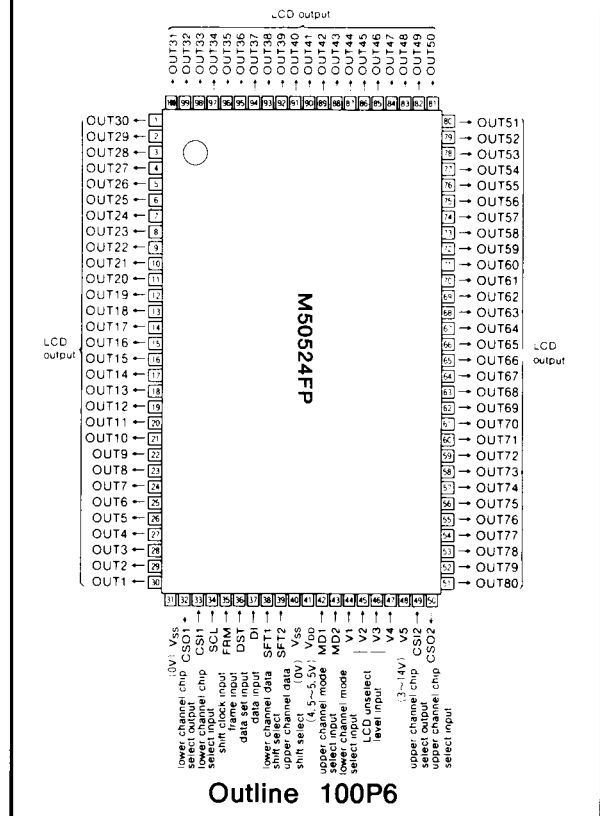
**FEATURES**

- Serial data input
- Two sets of built-in 40-channel liquid crystal drive circuits (total of 80 channel outputs)
- Two sets of drive circuits that can be used for either common or column types
- Two sets of drive circuits that can separately choose individual directions for data transfer
- The system's power consumption during data transfer can be reduced by chip selection
- Power supply of +5V (TYP) for internal logic circuit
- Power supply of +14V(MAX) for the liquid crystal drive circuit
- It is possible to interface directly with M50530-XXXXP (LCD CONTROLLER-DRIVER)

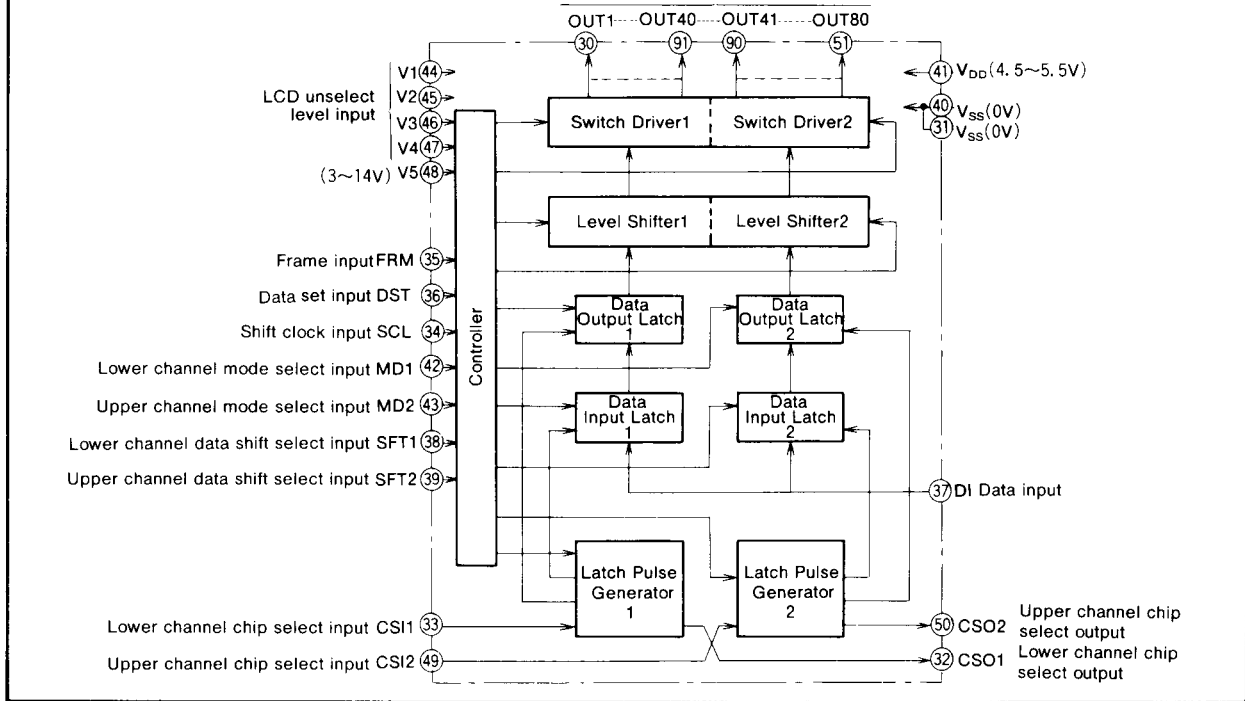
**APPLICATION**

OA apparatus (portable personal computer, electrical typewriter e.t.c) Information apparatus (Telephone, Fax e.t.c.)

**PIN CONFIGURATION (TOP VIEW)**



**BLOCK DIAGRAM**



80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER

**FUNCTIONAL DESCRIPTION**

M50524FP is the LCD driver IC. It has two internal 40-bit drive circuits, which select column mode or common mode through mode select (MD). Also, data shift direction is selected by data shift select (SFT).

In column drive mode, serial display input data is stored with the falling edge of the shift clock (SCL) signal.

The column LCD signal waveform is altered through the

level shifter and switch driver, and output with the raising edge of the data set (DST) signal.

In common drive mode, the LCD signal waveform is altered as above. This common data signal is then shifted with the raising edge of the data set (DST) signal.

Further more, in both modes, data is input and output with the chip select (CSI) signal.

**TERMINAL DESCRIPTION**

Pin	Name	I/O	Function																								
V <sub>DD</sub>	Power supply(Logic)	—	Power supply for logic circuit(+5V TYP)																								
V <sub>SS</sub>	Power supply(GND)	—	0V(Selected level of liquid crystal drive)																								
V5	Power supply(LCD)	—	Power supply for liquid crystal drive circuit(selected level)																								
V1~V4	Power supply(LCD)	—	Power supply for driving liquid crystal(non-selected level)																								
OUT1~OUT40	Liquid crystal output	O	Liquid crystal drive output(lower channels)																								
OUT41~OUT80	Liquid crystal output	O	Liquid crystal drive output(upper channels)																								
MD1	Lower channel mode selector	I	Selects operating modes for the lower channels(OUT1~OUT40). <table border="1" style="margin-left: 20px;"> <tr> <th>MD1</th> <th>Operating Mode</th> </tr> <tr> <td>H</td> <td>Column mode</td> </tr> <tr> <td>L</td> <td>Common mode</td> </tr> </table>	MD1	Operating Mode	H	Column mode	L	Common mode																		
MD1	Operating Mode																										
H	Column mode																										
L	Common mode																										
MD2	Upper channel mode selector	I	Selects operating modes for the upper channels(OUT41~OUT80). <table border="1" style="margin-left: 20px;"> <tr> <th>MD2</th> <th>Operating Mode</th> </tr> <tr> <td>H</td> <td>Column mode</td> </tr> <tr> <td>L</td> <td>Common mode</td> </tr> </table>	MD2	Operating Mode	H	Column mode	L	Common mode																		
MD2	Operating Mode																										
H	Column mode																										
L	Common mode																										
SFT1	Lower channel data shift selector	I	In column mode, when serial data is input in the order D1→D2→...→D40, determines the relationship between the data and the liquid crystal driver output(OUT)as follows. <table border="1" style="margin-left: 20px;"> <tr> <th>SFT1</th> <th>OUT1</th> <th>OUT2</th> <th>OUT3</th> <th>.....</th> <th>OUT40</th> </tr> <tr> <td>H</td> <td>D1</td> <td>D2</td> <td>D3</td> <td>.....</td> <td>D40</td> </tr> <tr> <td>L</td> <td>D40</td> <td>D39</td> <td>D38</td> <td>.....</td> <td>D1</td> </tr> </table> <p>In common mode, selects shift direction of selected scanning signal as follows.</p> <table border="1" style="margin-left: 20px;"> <tr> <th>SFT1</th> <th>Shift Direction of Selected Scanning Signal</th> </tr> <tr> <td>H</td> <td>OUT1→OUT2→OUT3 .....→OUT40</td> </tr> <tr> <td>L</td> <td>OUT40→OUT39→OUT38 .....→OUT1</td> </tr> </table>	SFT1	OUT1	OUT2	OUT3	.....	OUT40	H	D1	D2	D3	.....	D40	L	D40	D39	D38	.....	D1	SFT1	Shift Direction of Selected Scanning Signal	H	OUT1→OUT2→OUT3 .....→OUT40	L	OUT40→OUT39→OUT38 .....→OUT1
SFT1	OUT1	OUT2	OUT3	.....	OUT40																						
H	D1	D2	D3	.....	D40																						
L	D40	D39	D38	.....	D1																						
SFT1	Shift Direction of Selected Scanning Signal																										
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L	OUT40→OUT39→OUT38 .....→OUT1																										
SFT2	Upper channel data shift selector	I	In column mode, when serial data is input in the order D1→D2→...→D40, determines the relationship between the data and the liquid crystal driver output(OUT)as follows. <table border="1" style="margin-left: 20px;"> <tr> <th>SFT2</th> <th>OUT41</th> <th>OUT42</th> <th>OUT43</th> <th>.....</th> <th>OUT80</th> </tr> <tr> <td>H</td> <td>D1</td> <td>D2</td> <td>D3</td> <td>.....</td> <td>D40</td> </tr> <tr> <td>L</td> <td>D40</td> <td>D39</td> <td>D38</td> <td>.....</td> <td>D1</td> </tr> </table> <p>In common mode, determines shift direction of selected scanning signal as follows.</p> <table border="1" style="margin-left: 20px;"> <tr> <th>SFT2</th> <th>Shift Direction of Selected Scanning Signal</th> </tr> <tr> <td>H</td> <td>OUT41→OUT42→OUT43 .....→OUT80</td> </tr> <tr> <td>L</td> <td>OUT80→OUT79→OUT78 .....→OUT41</td> </tr> </table>	SFT2	OUT41	OUT42	OUT43	.....	OUT80	H	D1	D2	D3	.....	D40	L	D40	D39	D38	.....	D1	SFT2	Shift Direction of Selected Scanning Signal	H	OUT41→OUT42→OUT43 .....→OUT80	L	OUT80→OUT79→OUT78 .....→OUT41
SFT2	OUT41	OUT42	OUT43	.....	OUT80																						
H	D1	D2	D3	.....	D40																						
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H	OUT41→OUT42→OUT43 .....→OUT80																										
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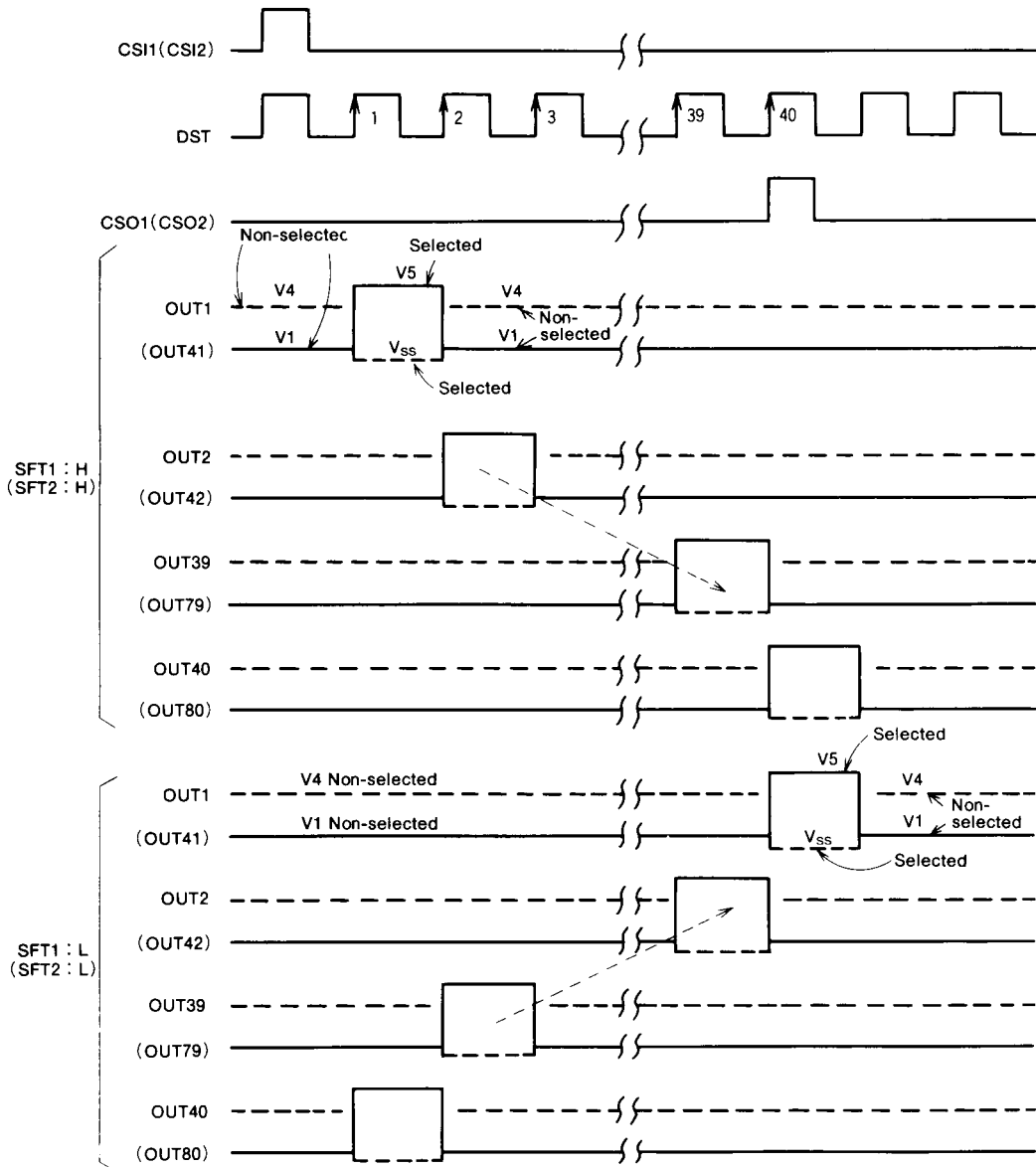
**80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER**

Pin	Name	I/O	Function																													
CSI1	Lower channel chip select input	I	Initializes control circuit for lower channels to activate circuit. Inputs positive pulse.																													
CSI2	Upper channel chip select input	I	Initializes control circuit for upper channels to activate circuit. Inputs positive pulse.																													
CSO1, CSO2	Chip select output	O	Used for cascade connection to expand number of liquid crystal driving channels. Connected to chip select input(CSI1 or CSI2)of expanded channel in next stage. CSO1 : Lower channel chip select output CSO2 : Upper channel chip select output																													
DI	Data input	I	Serial data input in column mode. Data is accepted into the Data Input Latch synchronized with SCL. Input data "1" (logic H level)and "0" (logic L level)correspond to selected data and non-selected data. Order of acceptance of input data (D1→D2...→D40), (that is at which OUT terminal it is to be output) is determined by SFT1 and SFT2. Common to upper and lower channels, and fixed in both cases to H or L when used in common mode.																													
SCL	Shift clock	I	Clock for accepting serial data into Input Latch. The data is taken in synchronization with the fall of SCL. When used in common mode, it is fixed to H or L for both upper and lower channels.																													
DST	Data set	I	In column mode, data is transferred from Data Input Latch to Data Output Latch in synchronization with rise of DST. In common mode, content of the Data Output Latch is shifted in synchronization with rise of DST. Shift direction is determined by SFT1 and SFT2. For both column and common modes, data is output to liquid crystal drive output(OUT)in synchronization with rise of DST.																													
FRM	Frame	I	AC-convert signal of liquid crystal drive output. For FRM, output level is selected as follows. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="3" rowspan="2"></th> <th colspan="2">FRM</th> </tr> <tr> <th>L</th> <th>H</th> </tr> </thead> <tbody> <tr> <td rowspan="2" style="text-align: center;">MD1 /</td> <td>L</td> <td>Common mode</td> <td>Selected output</td> <td>V<sub>SS</sub></td> <td>V5</td> </tr> <tr> <td></td> <td></td> <td>Non-selected output</td> <td>V4</td> <td>V1</td> </tr> <tr> <td rowspan="2" style="text-align: center;">MD2 /</td> <td>H</td> <td>Column mode</td> <td>Data 1 Selected output</td> <td>V5</td> <td>V<sub>SS</sub></td> </tr> <tr> <td></td> <td></td> <td>Data 0 Non-selected output</td> <td>V3</td> <td>V2</td> </tr> </tbody> </table> <p>For the above, assume that <math>V5 &gt; V4 \geq V3 \geq V2 \geq V1 &gt; V_{SS}</math></p>				FRM		L	H	MD1 /	L	Common mode	Selected output	V <sub>SS</sub>	V5			Non-selected output	V4	V1	MD2 /	H	Column mode	Data 1 Selected output	V5	V <sub>SS</sub>			Data 0 Non-selected output	V3	V2
			FRM																													
			L	H																												
MD1 /	L	Common mode	Selected output	V <sub>SS</sub>	V5																											
			Non-selected output	V4	V1																											
MD2 /	H	Column mode	Data 1 Selected output	V5	V <sub>SS</sub>																											
			Data 0 Non-selected output	V3	V2																											

**80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER**

**COMMON MODE TIME CHART**

MD1 (MD2) : L

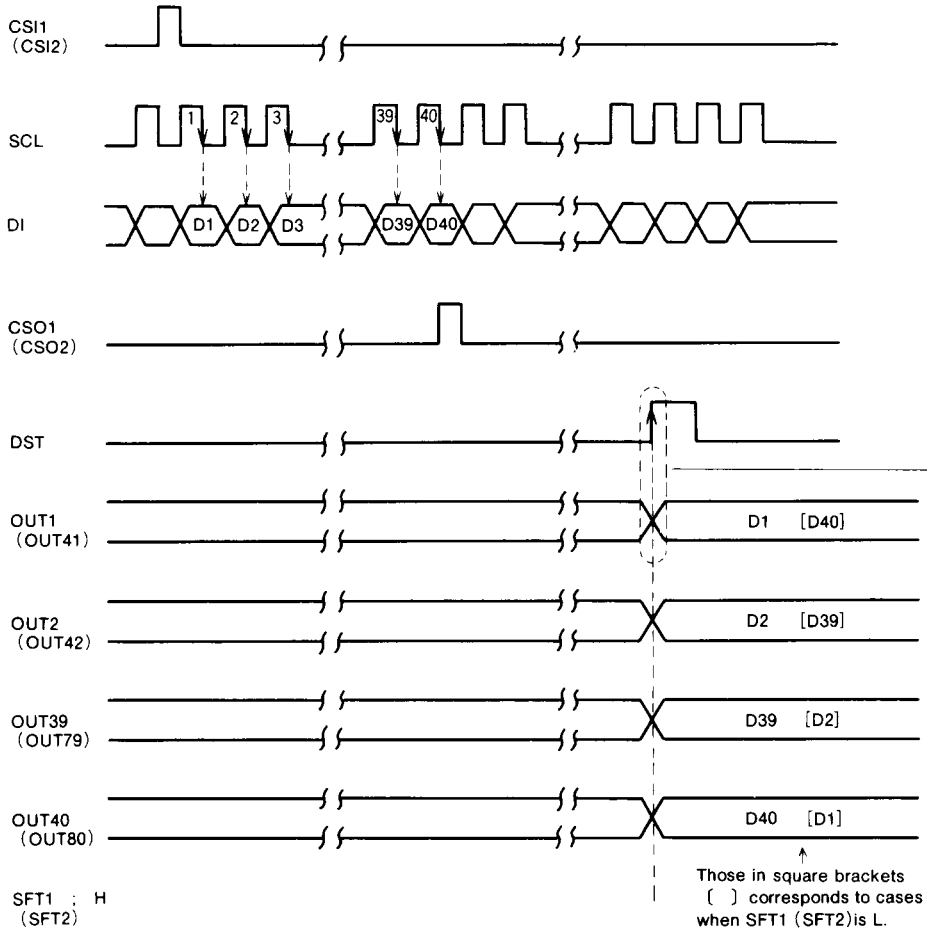


(Note) In the above diagram for OUT's, a solid line (—) and a broken line (---) indicate H and L levels, respectively, of the FRM.

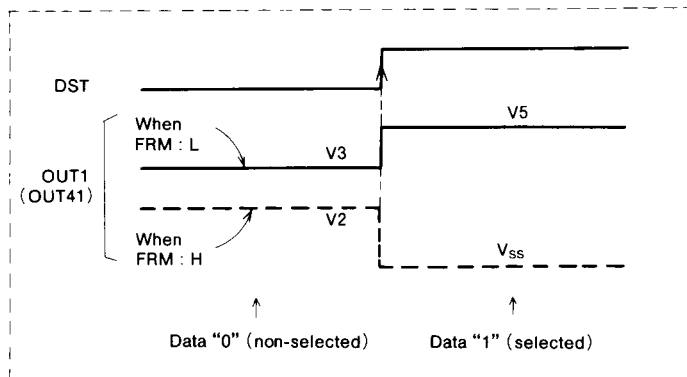
80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER

COLUMN MODE TIME CHART

MD1 (MD2) : H



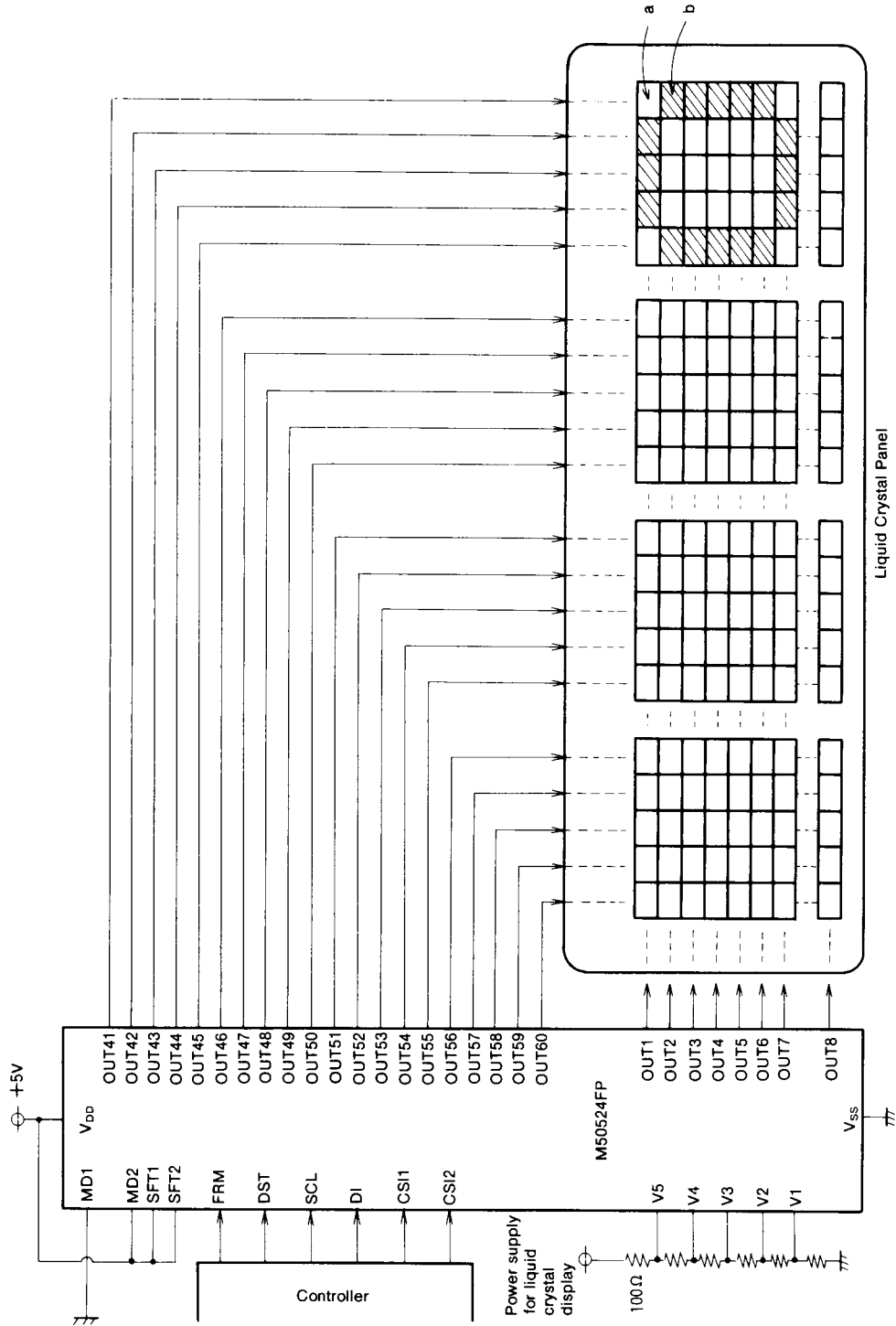
Examples of output waveform when data changes from 0 to 1 at OUT1(OUT41)



**80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER**

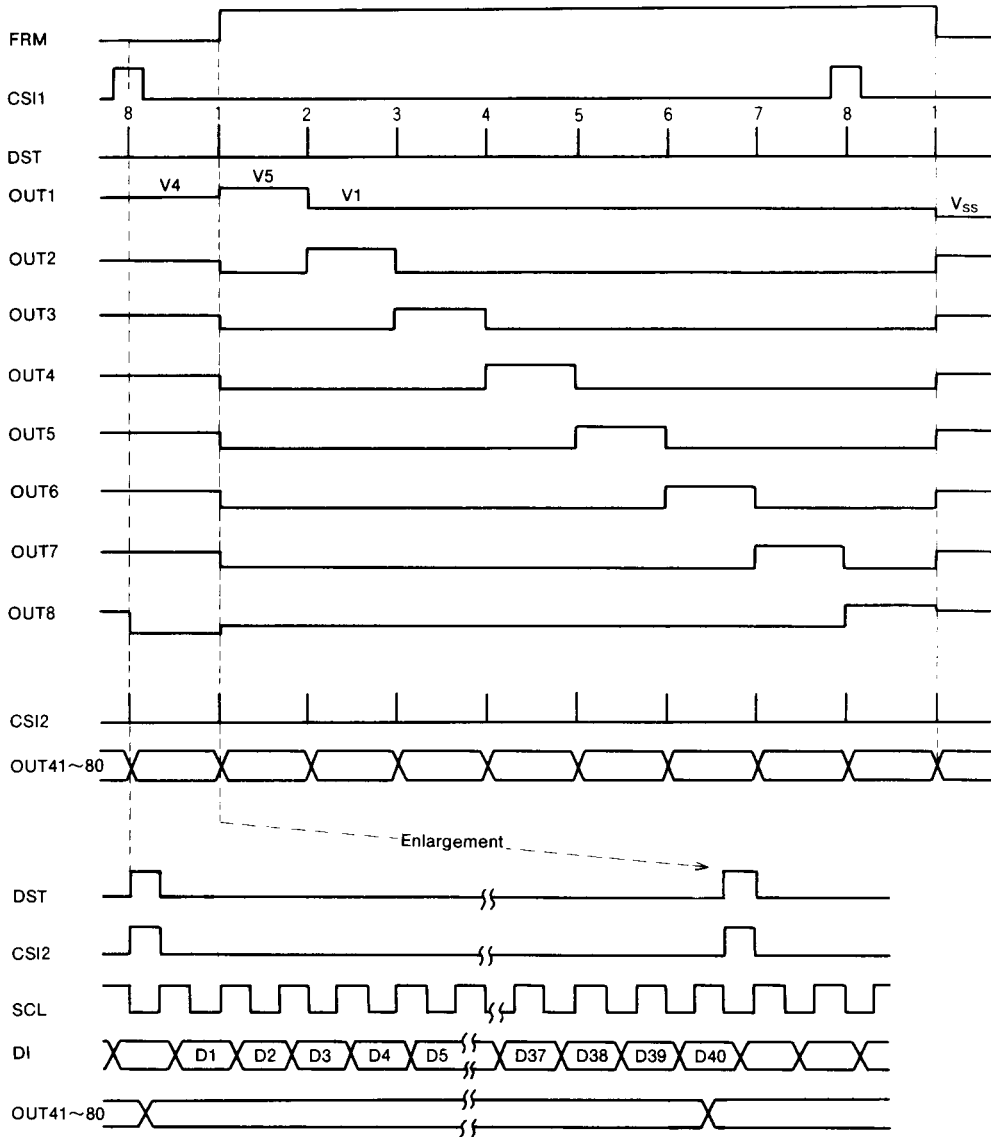
**M50524FP DRIVE EXAMPLES**

(1) Circuit example (5X8 dot 4-character display)



80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER

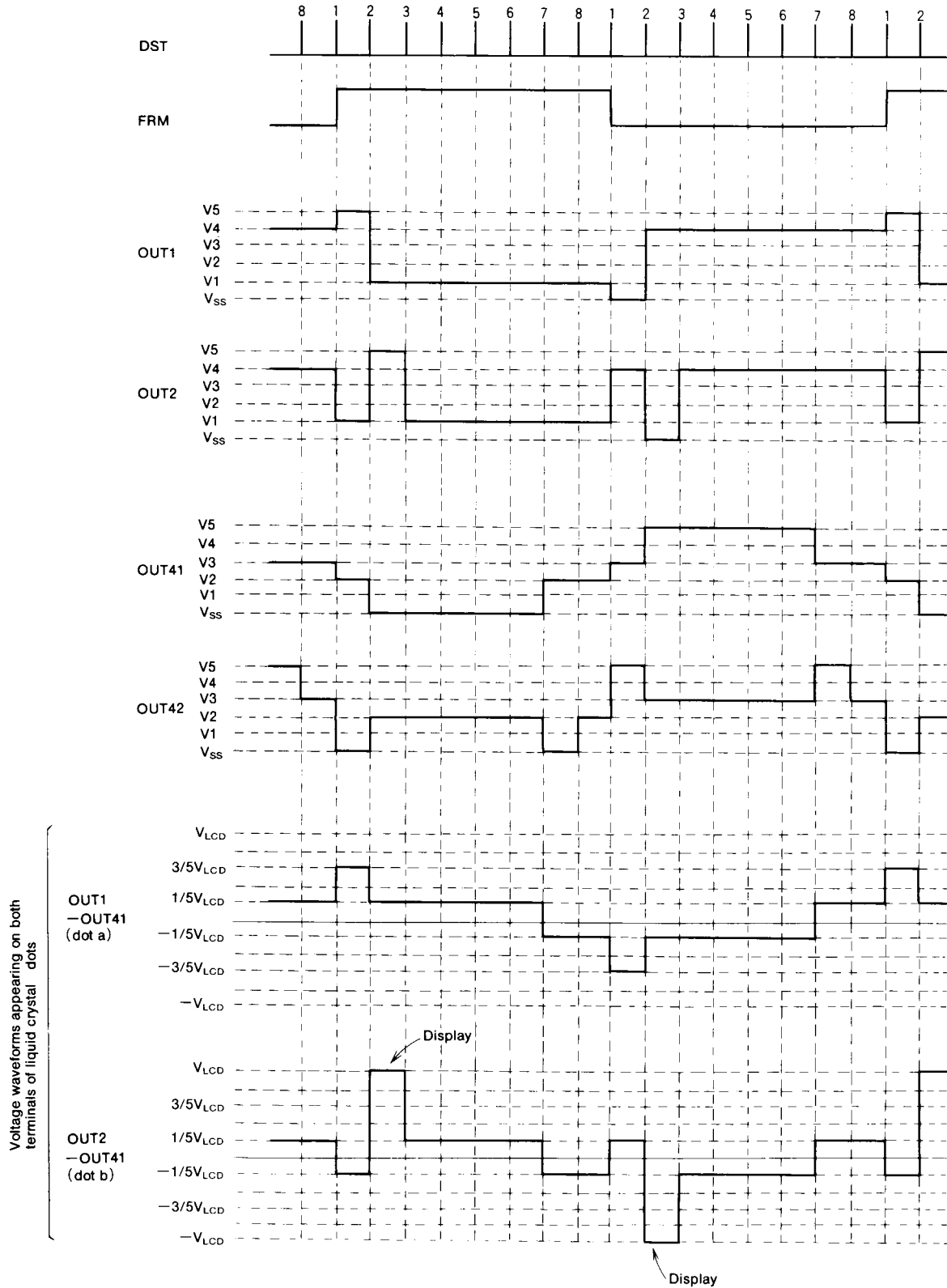
(2) Timing for various parts



In this example, the lower channels (OUT1~OUT40) are used as common drive and the upper channels (OUT41~80) are used as column drive. For OUT41~OUT80, only the timings for switching over output are indicated.

80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER

(3) Liquid crystal drive waveform





## 80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Ratings	Unit
$V_{DD}$	Supply voltage	Logic circuit		-0.3~+7	V
$V1\sim V5^*$		Liquid crystal drive circuit		-0.3~+15.0	V
$V_I$	Input voltage			$V_{SS}-0.3\leq V_I\leq V_{DD}+0.3$	V
$T_{opr}$	Ambient operating temperature			-20~+70	°C
$T_{stg}$	Storage temperature			-40~+125	°C
$P_d$	Maximum power consumption			300	mW

※ For the above, assume that  $V5 > V4 \geq V3 \geq V2 \geq V1$ .

RECOMMENDED OPERATING CONDITIONS ( $T_a = -20\sim+70^\circ\text{C}$ )

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{DD}$	Logic circuit supply voltage	4.5	5.0	5.5	V
$V5^*$	Liquid crystal drive circuit supply voltage	3		14	V
$V_{IL}$	"L" input voltage	$V_{SS}$	$V_{SS}$	$0.3 \times V_{DD}$	V
$V_{IH}$	"H" input voltage	$0.7 \times V_{DD}$	$V_{DD}$	$V_{DD}$	V

※ For  $V5$ , a resistor of not less than  $47\Omega (\pm 10\%)$  should be placed in sequence with the power supply.

ELECTRICAL CHARACTERISTICS (unless otherwise noted,  $V_{DD}=5\text{V}$  at  $T_a=25^\circ\text{C}$ )

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$I_{DD}$	Logic circuit supply current	$f_{SCL}=1.5\text{MHz}$			5	mA
$I_{V5}$	Liquid crystal drive circuit supply current	OUT1~80 No load $V5=14\text{V}$ $f_{DST}=4.8\text{kHz}$ , $f_{FRM}=30\text{Hz}$			100	$\mu\text{A}$
$V_{OL}$	"L" output voltage (CS01, CS02)	$I_{OL}=1.6\text{mA}$			0.4	V
$V_{OH}$	"H" output voltage (CS01, CS02)	$I_{OH}=-1.6\text{mA}$	3.5			V
$R_{ON}$	ON-resistance for liquid crystal output (OUT1~OUT80)	$V5=14\text{V}$			500	$\Omega$
		$V5=5\text{V}$			2	$\text{k}\Omega$

COMMON MODE TIMING CHARACTERISTICS (unless otherwise noted,  $V_{DD}=5\text{V}$ ,  $T_a=25^\circ\text{C}$ )

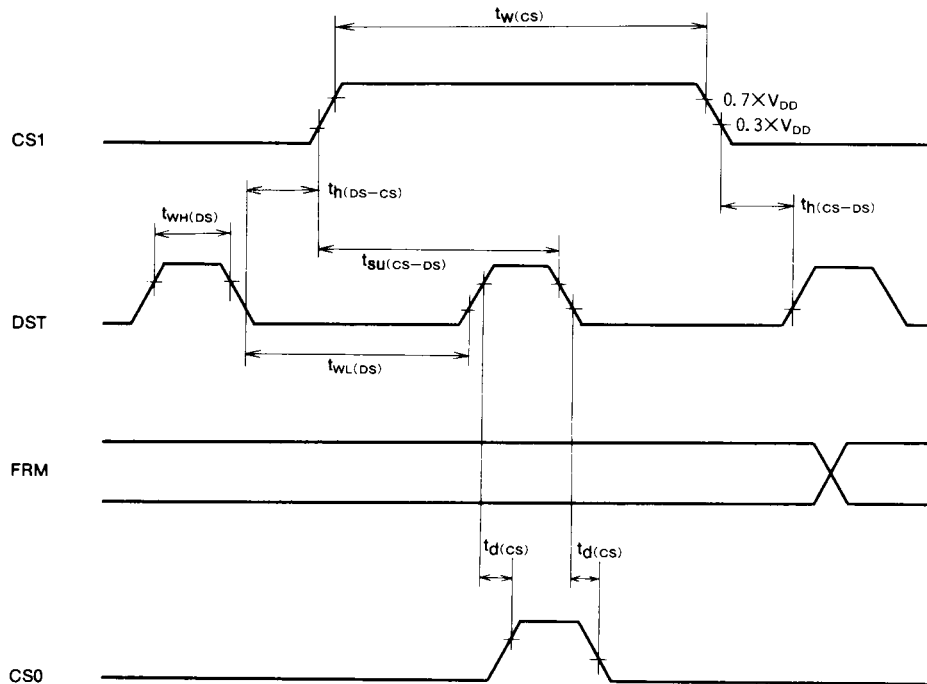
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(DS)}$	Data set "H" pulse width		500			ns
$t_{WL(DS)}$	Data set "L" pulse width		500			ns
$t_{h(DS-CS)}$	Chip select hold time		200			ns
$t_{su(CS-DS)}$	Chip select set-up time		300			ns
$t_{h(CS-DS)}$	Data set hold time		200			ns
$t_{w(CS)}$	Chip select pulse width		300			ns
$t_{d(CS)}$	Chip select delay time	$C_L=15\text{pF}$			300	ns

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COLUMN MODE TIMING CHARACTERISTICS (unless otherwise noted,  $V_{DD}=5V$  at  $T_a=25^\circ C$ )

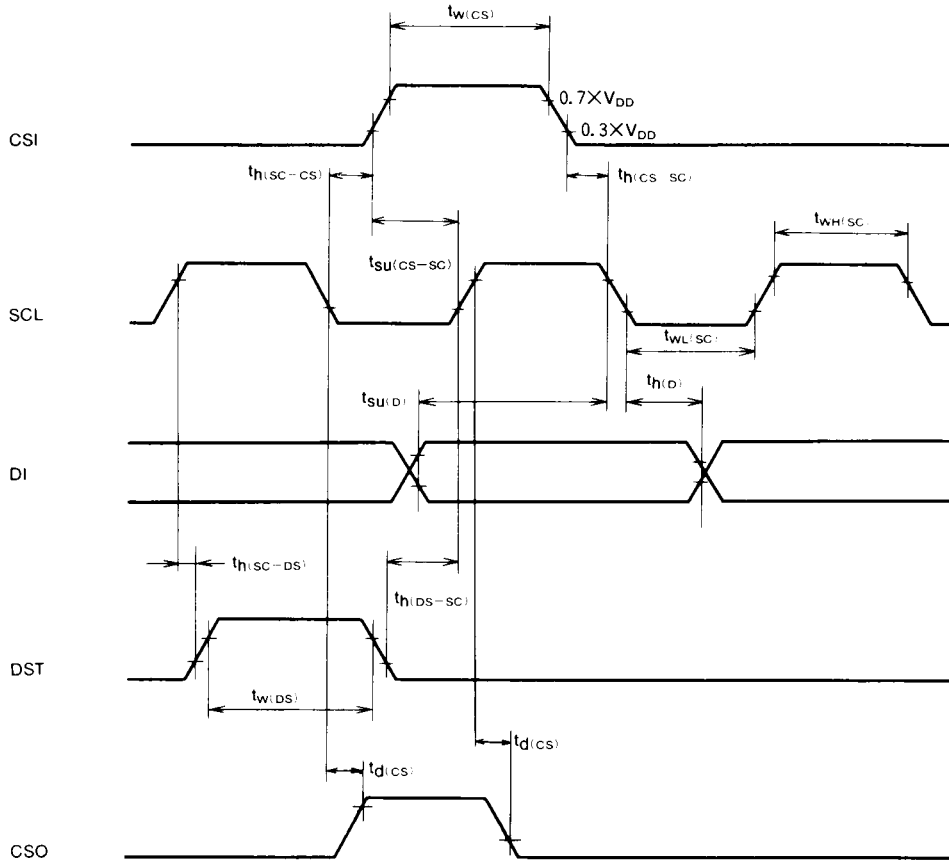
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{WH(SC)}$	Shift clock "H" pulse width		200			ns
$t_{WL(SC)}$	Shift clock "L" pulse width		200			ns
$f_{C(SC)}$	Shift clock frequency				2	MHz
$t_{H(SC-CS)}$	Chip select hold time		200			ns
$t_{SU(CS-SC)}$	Chip select set-up time		300			ns
$t_{H(CS-SC)}$	Shift clock hold time		200			ns
$t_{W(CS)}$	Chip select pulse width		300			ns
$t_{H(SC-DS)}$	Data set hold time		200			ns
$t_{H(DS-SC)}$	Shift clock hold time		200			ns
$t_{W(DS)}$	Data set pulse width		500			ns
$t_{SU(D)}$	Data set-up time		200			ns
$t_{H(D)}$	Data hold time		200			ns
$t_{d(CS)}$	Chip select output delay time	$C_L=15pF$			300	ns

COMMON MODE TIMING WAVEFORM



80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER

COLUMN MODE TIMING WAVEFORM



80CHANNEL OUTPUT LIQUID CRYSTAL DISPLAY DRIVER

SYSTEM CONNECTION EXAMPLE

