élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2252C

Dual 50 MHz Comparator/Pin Receiver

Features

- Fast response—7 ns
- Inputs tolerate large overdrives with no speed nor bias current penalties
- Propagation delay is relatively constant with variations of input Slew Rate, overdrive, temperature, and supply voltage
- Output provides proper CMOS or TTL logic levels
- Hysteresis is available on-chip
- Large voltage gain—8000 V/V
- Not oscillation-prone
- Can detect 4 ns glitches
- MIL-STD-883 Rev. C compliant

Applications

- Pin receiver for automatic test equipment
- Data communications line receiver
- Frequency counter input
- Pulse squarer

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2252CN	0°C to +75°C	14-Pin P-DIP	MDP0031
EL2252CM	0°C to +75°C	20-Lead SOL	MDP0027

General Description

The EL2252 dual comparator replaces the traditional input buffer + attenuator + ECL comparator + ECL to TTL translator circuit blocks used in digital equipment. The EL2252 provides a quick 7 ns propagation delay while complying with ±10V inputs. Input accuracy and propagation delay is maintained even with input signal Slew Rates as great as 4000 V/μs. The EL2252 can run on supplies as low as −5.2V and +9V and comply with ECL and CMOS inputs, or use supplies as great as ±18V for much greater input range.

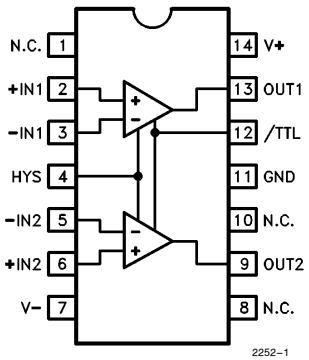
The EL2252 has a /TTL pin which, when grounded, restricts the output V_{OH} to a TTL swing to minimize propagation delay. When left open, the output V_{OH} increases to a valid CMOS level.

The comparators are well behaved and have little tendency to oscillate over a variety of input and output source and load impedances. They do not oscillate even when the inputs are held in the linear range of the device. To improve output stability in the presence of input noise, an internal 60 mV of hysteresis is available by connecting the HYS pin to V−.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see Elantec document, QRA-1; "*Elantec's Processing, Monolithic Integrated Circuits*".

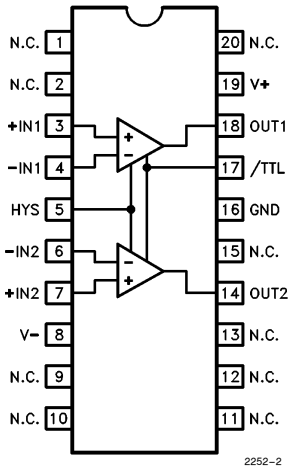
Connection Diagrams

14-Pin DIP



Top View

20-Pin SOL



Top View

December 1995 Rev E

Absolute Maximum Ratings (T_A = 25°C)

Voltage between V+ and V−	36V	Internal Power Dissipation	See Curves
Voltage at V+	18V	Operating Ambient Temperature Range	−25°C to +85°C
Voltage between −IN and +IN pins	36V	Operating Junction Temperature	150°C
Output Current	12 mA	Storage Temperature Range	−65° to +150C
Current into +IN, −IN, HYS or /TTL	5 mA		

Important Note:

All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

DC Electrical Characteristics V_S = ±15V; HYS and /TTL grounded; T_A = 25°C unless otherwise specified

Parameter	Description	Temp	Min	Typ	Max	Test Level EL2252C	Units
V_{OS}	Input Offset Voltage	25°C		1	9	I	mV
		Full			13	III	mV
TCV_{OS}	Average Offset Voltage Drift	Full		7		V	µV/C
I_B	Input Bias Current at Null	25°C		6	16	I	µA
		Full			21	III	µA
I_{OS}	Input Offset Current	25°C		0.2	1	I	µA
		Full			2	III	µA
R_{IN}, diff	Input Differential Resistance	25°C		30		V	kΩ
R_{IN}, comm	Input Common-Mode Resistance	25°C		10		V	MΩ
C_{IN}	Input Capacitance	25°C		2		V	pF
$V_{CM}+$	Positive Common-Mode Input Range	Full	10	13		II	V
$V_{CM}-$	Negative Common-Mode Input Range	Full	−9	−12		II	V
A_{VOL}	Large Signal Voltage Gain V_O = 0.8V to 2.0V	25°C	4000	8000		I	V/V
		Full	3000			III	V/V

TD is 3.3in

DC Electrical Characteristics

V_S = ±15V; HYS and /TTL grounded; T_A = 25°C unless otherwise specified — Contd.

Parameter	Description	Temp	Min	Typ	Max	Test Level EL2252C	Units
CMRR	Common-Mode Rejection Ratio (Note 1)	Full	70	95		II	dB
PSRR	Power-Supply Rejection Ratio (Note 2)	Full	70	90		II	dB
V_{HYS}	Peak-to-Peak Input Hysteresis with HYS connected to V−	25°C		60		V	mV
V_{OH}	High Level Output, CMOS Mode	Full	4.0	4.6	5.1	II	V
	TTL Mode	Full	2.4	2.7	3.2	II	V
V_{OL}	Low Level Output, I1 = 0	Full	−0.2	0.2	0.8	II	V
	I1 = 5 mA	Full	−0.2	0.4	0.8	II	V
I_S+	Positive Supply Current	Full		16	19	II	mA
I_S-	Negative Supply Current	Full		17	20	II	mA

AC Electrical Characteristics

V_S = ±15V; C_L = 10 pF; T_A = 25°C; TTL output threshold is 1.4V, CMOS output threshold is 2.5V; unless otherwise specified

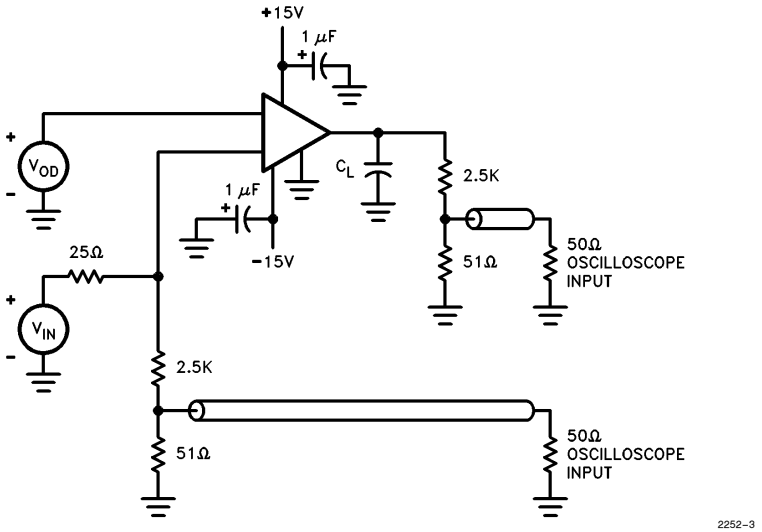
Parameter	Description	Min	Typ	Max	Test Level EL2252C	Units
T_{PD+}, T_{PD-}	Input to Output Propagation Delay, 0 < V_{IN} < 5V, 500 mV Overdrive, 2000 V/µs Input Slew Rate TTL Output Swing		6	9	III	ns
	CMOS Output Swing		8		V	ns
T_{PD+}, T_{PD-}	Input to Output Propagation Delay, −2V < V_{IN} < −1V, 500 mV Overdrive, 2 ns Input Rise Time TTL Output Swing		5	9	III	ns
	CMOS Output Swing		9		V	ns
T_{PDSYM}	Propagation Delay Change between Positive and Negative Input Slopes		1.25		V	ns

Note 1: Two tests are performed with V_{CM} = 0V to −9V and V_{CM} = 0V to 10V.
Note 2: Two tests are performed with V+ = 15V, V− changed from −10V to −15V; V− = −15V, V+ changed from 10V to 15V.

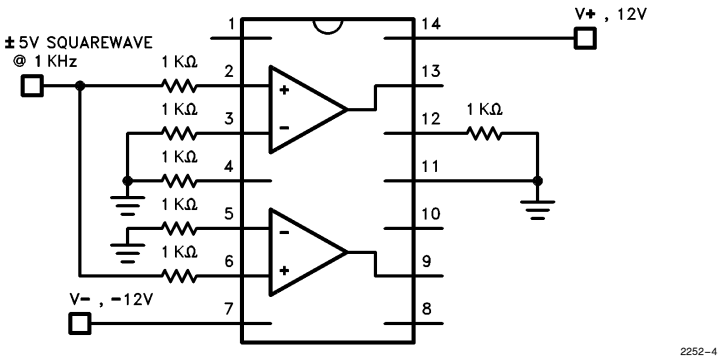
TD is 2.5in

TD is 2.2in

AC Test Circuit

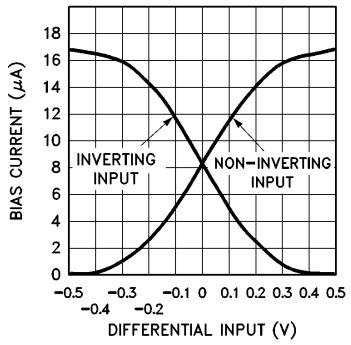


Burn-In Circuit

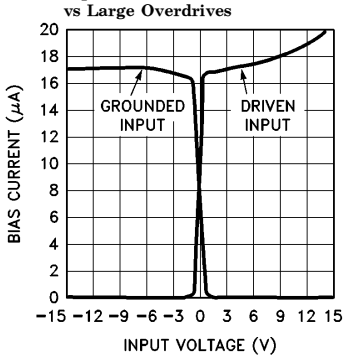


Typical Performance Curves

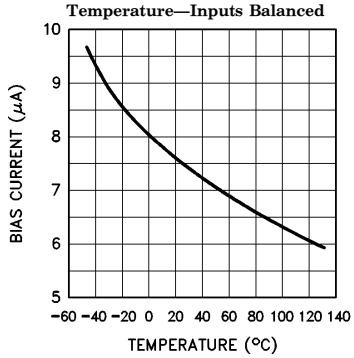
Input Bias Current vs Small Overdrives



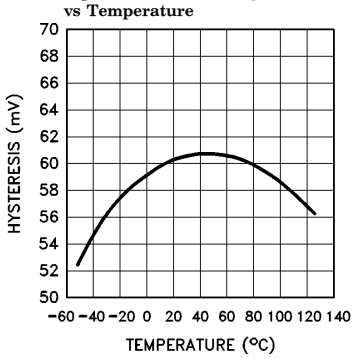
Input Bias Current vs Large Overdrives



Bias Current vs Temperature—Inputs Balanced

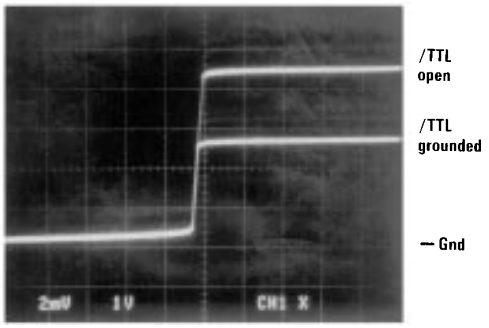


Input Hysteresis Voltage vs Temperature



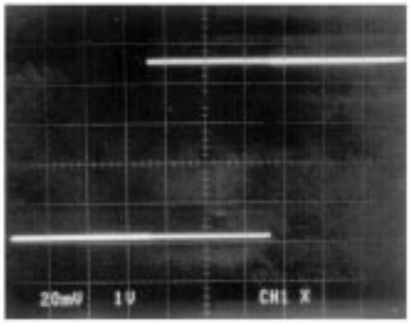
2252-5

Input/Output Transfer Function—HYS Open



2252-6

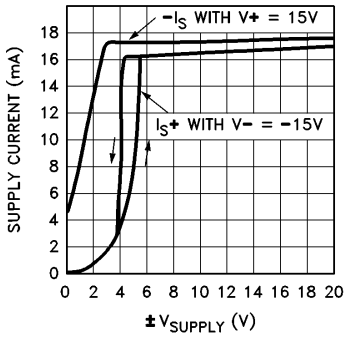
Input/Output Transfer Function—HYS Connected to V



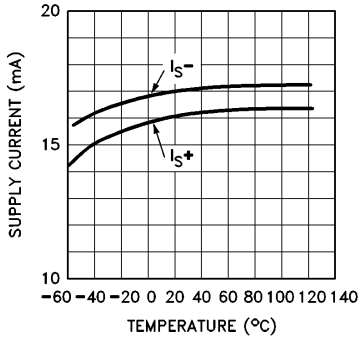
2252-7

Typical Performance Curves — Contd.

Supply Current vs Supply Voltage

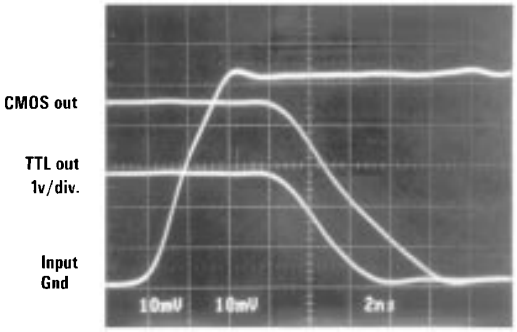


Supply Current vs Temperature (V_S = ±15V)



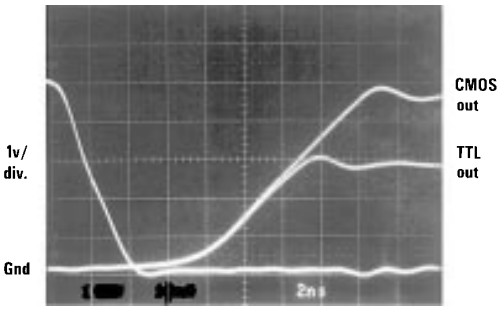
2252-8

Output Delay—0.5V Overdrive



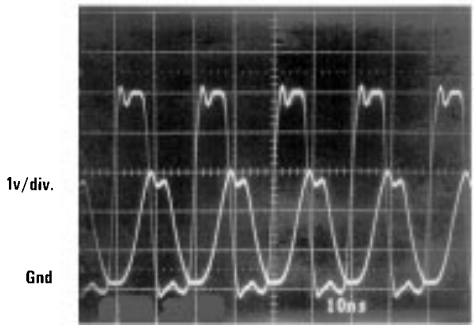
2252-9

Output Delay—0.5V Overdrive



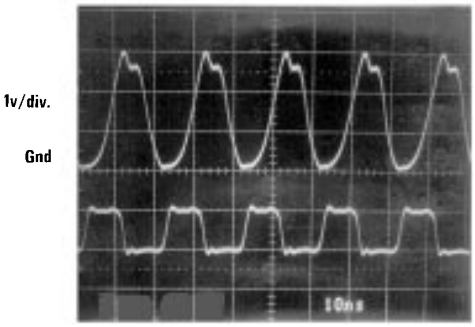
2252-10

Output with 50 MHz CMOS Input



2252-11

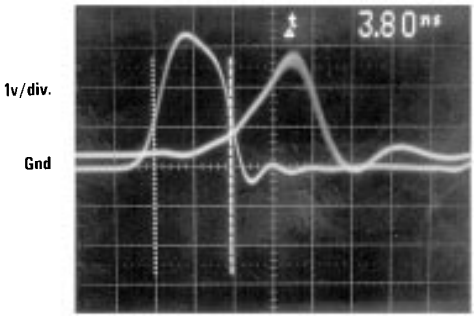
Output with 50 MHz ECL Input



2252-12

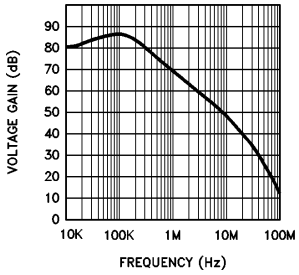
Typical Performance Curves — Contd.

4 ns TTL Glitch Detection

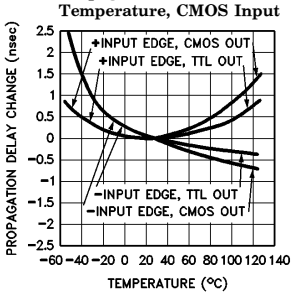


2252-13

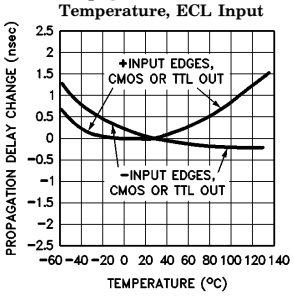
Gain vs Frequency



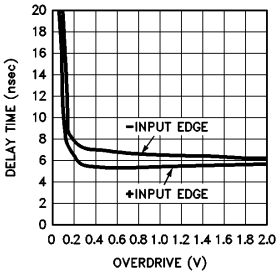
Propagation Delay vs Temperature, CMOS Input



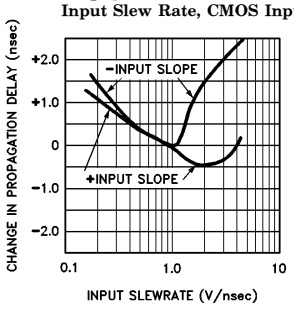
Propagation Delay vs Temperature, ECL Input



Propagation Delay vs Overdrive, CMOS Input



Propagation Delay vs Input Slew Rate, CMOS Input



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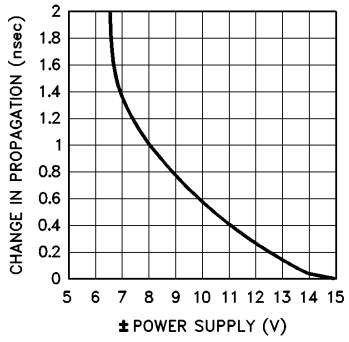
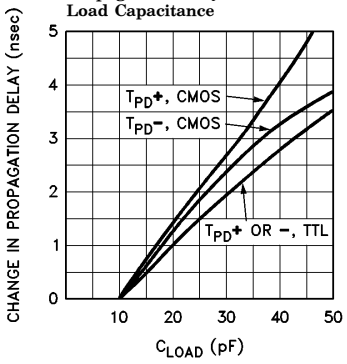
Typical Performance Curves — Contd.

Propagation Delay vs Power Supply Voltage

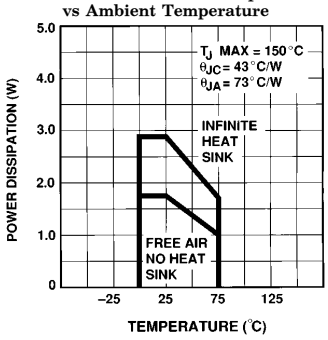


Propagation Delay vs Load Capacitance



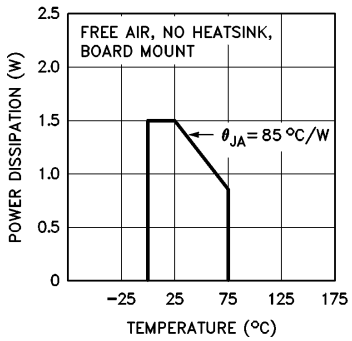
2252-15

14-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



2252-16

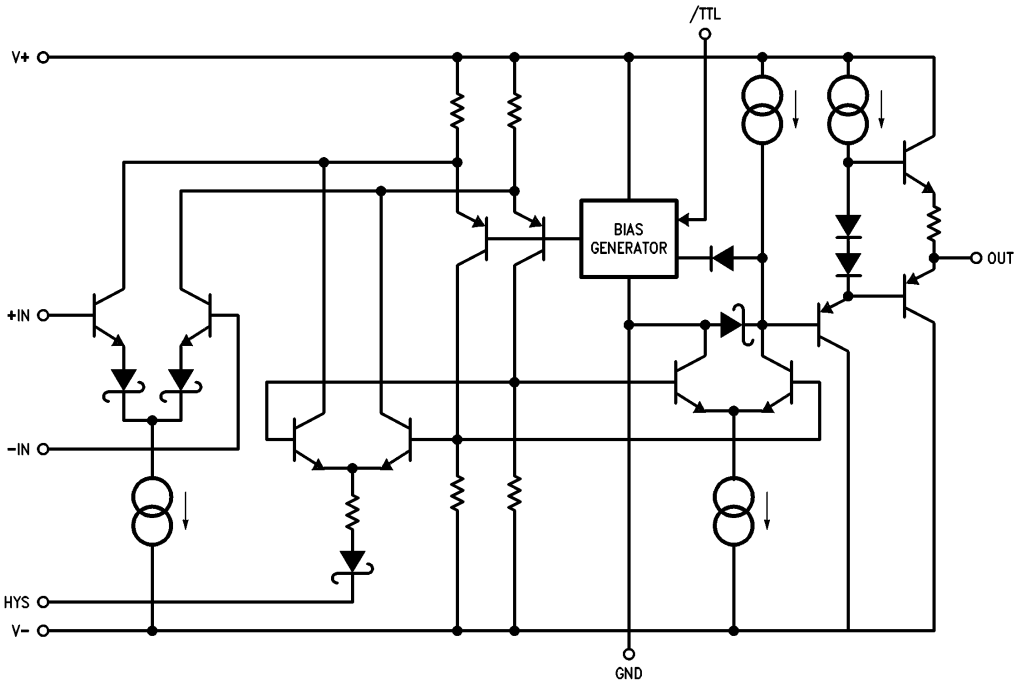
20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



2252-18

Simplified Schematic

One Comparator



2252−19

Applications Information

The EL2252 is very easy to use and is relatively oscillation-free, but a few items must be attended. The first is that both supplies should be bypassed closely. 1 μF tantalums are very good and no additional smaller capacitors are necessary. The EL2252 requires V− to be at least 5V to preserve AC performance. V+ must be at least 6V for a TTL output swing, 8V for CMOS outputs.

The input voltage range will be referred to the more positive of the two inputs. That is, bringing an input as negative as V− will not cause problems; it's the other input's level that must be considered. The typical input range is +13/−12V when the supplies are ±15V. This range diminishes over temperature and varies with processing; it is wise to set power supplies such that V+ is 5V more positive than the most positive input signal and V− more negative than 6V below the most negative input. ±12V supplies will easily encompass all CMOS and ECL logic inputs. If the input exceeds the device's common-mode input capability, the EL2252 propagation delay and input bias current will increase. Fault currents will occur with inputs a diode below V− or above V+. No damage nor V_{OS} shift will occur even when fault currents within the absolute maximum ratings.

Applications Information — Contd.

One of the few ways in which oscillations can be induced is by connecting a high-Q reactive source impedance to the EL2252 inputs. Such sources are long wires and unterminated coaxial lines. The source impedance should be de-Q'ed. One method is to connect a series resistor to the EL2252 input of around 100Ω value. More resistance will calm the system more effectively, but at the expense of comparator response time. Another method is to install a "snubber" network from comparator input to ground. A snubber is a resistor in series with a small capacitor, around 100Ω and 33 pF. Each physical and electrical environment will require different treatments, although many need none.

The major use of the HYS pin is to suppress noise superimposed on the input signal. By shorting the HYS pin to V^- a ±30 mV hysteresis is placed around the V_{OS} of the comparator input. Leaving the pin open, or more appropriately, grounding the HYS pin removes all hysteresis. Connecting a resistor between HYS and V^- allows an adjustment of the peak-to-peak hysteresis level. Unfortunately, an external resistor cannot track the internal devices properly, so temperature and unit-to-unit variations of hysteresis are increased. The relationship between the resistor and resulting hysteresis level is not linear, but a 1.5k resistor will approximately halve the nominal value.

The time delay of the EL2252 will increase by about 0.7 ns when using full hysteresis.

The EL2252 is specifically designed to be tolerent of large inputs. It will exhibit very much increased delay times for input overdrives below 100 mV. If very small overdrives must be sensed, the EL2018 or EL2019 comparators would be good choices, although they lose accuracies with signal input Slew Rates above 400 V/µs. The EL2252 keeps its timing accuracy with input Slew Rates between 100 V/µs and 4000 V/µs of input Slew Rate.

The output stage drives tens of pF load capacitances without increased overshoot, but propagation delay increases about 1 ns per 10 pF. The output circuit is not a traditional TTL stage, and using an external pullup resistor will not change the V_{OH}. In general setting the output swing to TTL (by grounding the /TTL pin) will optimize overall propagation delay and ±swing symmetry.

EL2252C Macromodel

```
* Connections:      +input
*                   |      -input
*                   |      |      +V
*                   |      |      |      -V
*                   |      |      |      |      HYS
*                   |      |      |      |      |      TTL
*                   |      |      |      |      |      |      output
*                   |      |      |      |      |      |      |
.subckt M2252       2      3      14     7      4      5      13
*
* Application Hints:
*
* Connect pin 4 to ground through 1000 MΩ resistor to inhibit
* Hysteresis; to invoke Hysteresis, connect pin 4 to V-.
*
* Connect pin 5 to ground to invoke TTL VOH; pin 5 may left open
* for CMOS VOH.
*
* To facilitate .OP, set itl1 = 200, itl2 = 200, set node 27 to 13.8V,
* and node 30 to -12V.
*
*Input Stage
*
i1 22 7 1.7mA
r1 14 20 300
r2 14 21 300
q1 20  2 22 qn
q2 21  3 22 qn
q3 20 26 23 qn
q4 21 25 23 qn
q13 25 27 20 qp
q14 26 27 21 qp
v1 14 27 1.2V
r3 23 24 1.4k
d1 24 4 ds
r4 25 33 700
r5 26 33 700
q16 33 33 34 qn
q17 34 34 37 qn
v4 37 7 1.2V
*
* 2nd Stage
*
i2 30 7 3mA
i3 14 28 1.5mA
q7 0 35 28 qp
v2 44 0 1.2V
s1 44 35 5 0 swa
s2 45 35 5 0 swb
rsw 14 5 10k
```

EL2252C
Dual 50 MHz Comparator/Pin Receiver

EL2252C Macromodel — Contd.

```
v3 45 0 2.5V
q5 0 26 30 qn
q6 28 25 30 qn
d3 0 28 ds
*
* Output Stage
*
i4 14 38 1mA
q8 38 38 39 qn
q9 32 32 39 qp
q10 7 28 32 qp
q11 14 38 40 qn 2
q12 7 28 13 qp 2
r6 40 13 50
c1 28 0 3pF
*
* Models
*
.model qn npn (is=2e-15 bf=120 tf=0.2nS cje=0.2pF cjc=0.2pF ccs=0.2pF)
.model qp pnp (is=0.6e-15 bf=60 tf=0.2nS cje=0.5pF cjc=0.3pF ccs=0.2pF)
.model ds d(is=3e-12 tt=0.05nS eg=0.72V vj=0.58)
.model swa vswitch (von=0v voff=2.5V)
.model swb vswitch (von=2.5 voff=0V)
.ends
```


élantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

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