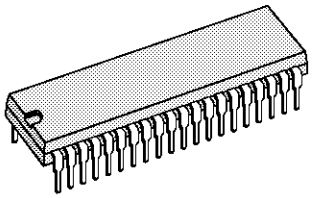
SGS-THOMSON MICROELECTRONICS

EF9345

HMOS2 SINGLE CHIP SEMI-GRAPHIC DISPLAY PROCESSOR

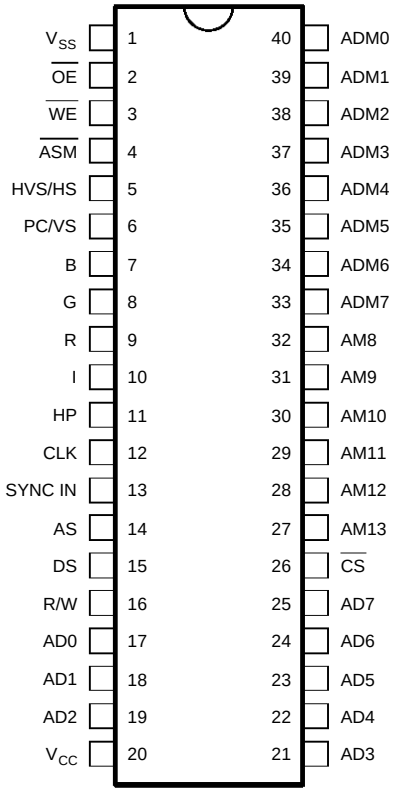
- SINGLE CHIP LOW-COST COLOR CRT CONTROLLER
- TV STANDARD COMPATIBLE (50Hz or 60Hz)
- 2 SCREEN FORMATS :
  - 25 (or 21) ROWS OF 40 CHARACTERS
  - 25 (or 21) ROWS OF 80 CHARACTERS
- ON-CHIP 128 ALPHANUMERIC AND 128 SEMI-GRAPHIC CHARACTER GENERATOR TWO STANDARD OPTIONS AVAILABLE FOR ALPHANUMERIC SETS (EF9345-R003 IS NO MORE AVAILABLE)
- EASY EXTENSION OF USER DEFINED ALPHANUMERIC OR SEMI-GRAPHIC SETS (> 1 K CHARACTERS)
- 40 CHARACTERS/ROW ATTRIBUTES : FOREGROUND AND BACKGROUND COLOR, DOUBLE HEIGHT, DOUBLE WIDTH, BLINKING, REVERSE, UNDERLINING, CONCEAL, INSERT, ACCENTUATION OF LOWER CASE CHARACTERS
- 80 CHARACTERS/ROW ATTRIBUTES : UNDERLINING, BLINKING, REVERSE, COLOR SELECT
- PROGRAMMABLE ROLL-UP, ROLL-DOWN AND CURSOR DISPLAY
- ON-CHIP R, G, B, I VIDEO SHIFT REGISTERS
- EASY SYNCHRONIZATION WITH EXTERNAL VIDEO-SOURCE : ON-CHIP PHASE COMPARATOR
- ADDRESS/DATA MULTIPLEXED BUS DIRECTLY COMPATIBLE WITH STANDARD MICROCOMPUTERS SUCH AS 6801, 6301, 8048, 8051, ST9
- ADDRESSING SPACE : 16K x 8 OF GENERAL PURPOSE PRIVATE MEMORY
- EASY OF USE OF ANY LOW-COST MEMORY COMPONENTS : ROM, SRAM, DRAM



DIP40
(Plastic Package)

ORDER CODE : EF9345P

PIN CONNECTIONS



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DESCRIPTION

The EF9345, new advanced color CRT controller, in conjunction with an additional standard memory package allow full implementation of the complete display control unit of a color or monochrome low-cost termainl, thus significantly reducing IC cost and PCB space.

PIN DESCRIPTION (All the input/output pins are TTL compatible)

Name	Pin Type	Pin N°	Function	Description
MICROPROCESSOR INTERFACE				
AD(0:7)	I/O	17-29 21-25	Multiplexed Address/Data Bus	These 8 bidirectional pins provide communication with the microprocessor system bus.
AS	I	14	Address Strobe	The falling edge of this control signal latches the address on the AD(0:7) lines, the state of the Data Strobe (DS) and Chip Select ($\overline{CS}$) into the chip.
DS	I	15	Data Strobe	When this input is strobed high by AS, the output buffers are selected while DS is low for a read cycle (R/$\overline{W}$ = 1). In write cycle, data present on AD(0:7) lines are strobed by R/$\overline{W}$ low (see timing diagram 2). When this input is strobed low by AS, R/$\overline{W}$ gives the direction of data transfer on AD(0:7) bus. DS high strobes the data to be written during a write cycle (R/$\overline{W}$ = 0) or enables the output buffers during a read cycle (R/$\overline{W}$ = 1). (see timing diagram 1).
R/$\overline{W}$	I	16	Read/Write	This input determines whether the Internal registers get written or read. A write is active low ("O").
$\overline{CS}$	I	26	Chip Select	The EF9345 is selected when this input is strobed low by AS.
MEMORY INTERFACE				
ADM(0:7)	I/O	40-43	Multiplexed Address/Data Bus	Lower 8 bits of memory address appear on the bus when $\overline{ASM}$ is high. It then becomes the data bus when ASM is low.
AM(8:13)	O	32-27	Memory Address Bus	These 6 pins provide the high order bits of the memory address.
$\overline{OE}$	O	2	Output Enable	When low, this output selects the memory data output buffers.
$\overline{WE}$	O	3	Write Enable	This output determines whether the memory gets read or written. A write is active low ("0").
$\overline{ASM}$	O	4	Memory Address Strobe	This signal cycles continuously. Address can be latched on its falling edge.
OTHER PINS				
CLK	I	12	Clock Input	External TTL clock Input (nominal value : 12MHz, duty cycle : 50%).
V_{SS}	S	1	Power Supply	Ground.
V_{CC}	S	20	Power Supply	+5V
VIDEO INTERFACE				
R G B	O O O	7 8 9	Red Green Blue	These outputs deliver the video signal. They are low during the vertical and horizontal blanking intervals.
I	O	10	Insert	This active high output allows to insert R : G: B : in an external video signal for captioning purposes, for example. It can also be used as a general purpose attribute or color.
HVS/HS	O	5	Sync. Out	This output delivers either the composite synchro (bit TGS_4 = 1) or the horizontal synchro signal (bit TGS_4 = 0)
PC/VS	O	6	Phase Comparator / Vertical Sync	When TGS_4 = 1, this signal is the phase comparator output. When TGS_4 = 0, this output delivers the vertical synchro signal.
SYNC IN	I	13	Synchro In	This input allows vertical and/or horizontal synchronizing the EF9345 on an external signal. It must be grounded if not used.
HP	O	11	Video Clock	This output delivers a 4MHz clock phased with the R, G, B, I signals.

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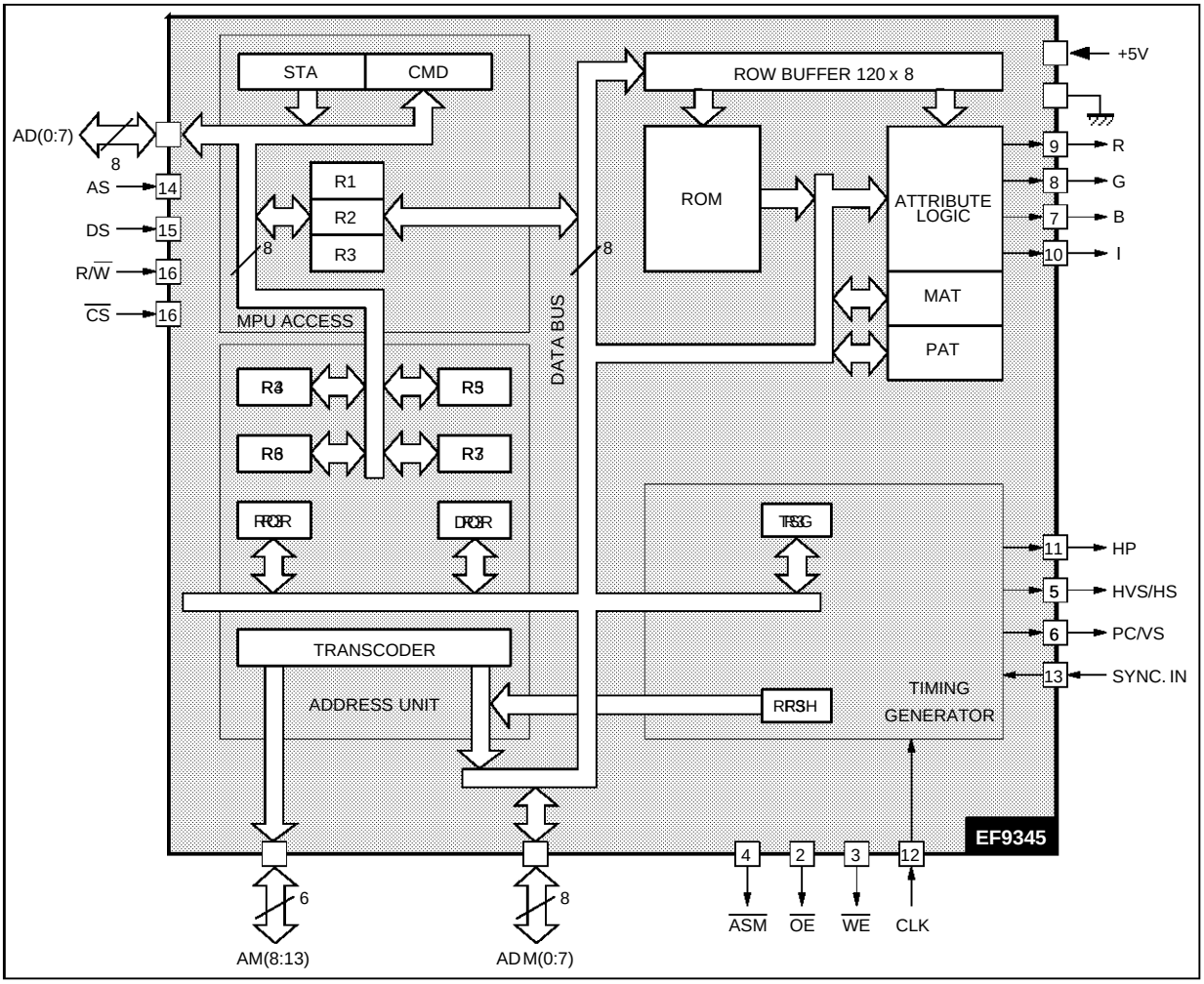
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}*	Supply Voltage	-0.3, 7.0	V
V_{in}*	Input Voltage	-0.3, 7.0	V
T_A	Operating Temperature	0, +70	^oC
T_{stg}	Storage Temperature	-55, +150	^oC
P_{Dm}	Maximum Power Dissipation	0.75	W

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* With respect to Vss.

Stresses above those hereby listed may cause permanent damage to the device. The ratings are stress ones only and functional operation of the device at these or any conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect reliability. Standard MOS circuits handling procedure should be used to avoid possible damage to the device.

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±5%, V_{SS} = 0V, T_A = 0 to +70°C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{IH}	Input High Voltage : CLK Other Inputs	2.2 2		V_{CC} V_{CC}	V
I_{IN}	Input Leakage Current			10	µA
V_{OH}	Output High Voltage (I_{load} = -500µA)	2.4			V
V_{OL}	Output Low Voltage : I_{load} = 4mA ; AD(0:7), ADM(0:7), AM(8:13) I_{load} = 1mA ; Other Outputs	0.4 0.4			V
P_D	Power Dissipation		250		mW
C_{IN}	Input Capacitance			15	pF
I_{TSI}	Three State (Off State) Input Current			10	µA

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MEMORY INTERFACE

V_{CC} = 5.0V ±5%, T_A = 0 to + 70°C
Clock : f_{in} = 12MHz ; Duty Cycle 40 to 60% ; t_r, t_f < 5ns
Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V, V_{OL} = 0.4V and V_{OH} = 2.4V

Symbol	Ident. N°	Parameter	Min.	Typ.	Max.	Unit
t_{ELEL}	1	Memory Cycle Time		500		ns
t_D	2	Output Delay Time from CLK Rising Edge ($\overline{ASM}$, $\overline{OE}$, $\overline{WE}$)			60	ns
t_{EHEL}	3	ASM High Pule Width	120			ns
t_{ELDV}	4	Memory Access Time from $\overline{ASM}$ Low			290	ns
t_{DA}	5	Output Delay Time from CLK Rising Edge (ADM(0:7), AM(8:13))			80	ns
t_{AVEL}	6	Address Setup Time to $\overline{ASM}$	30			ns
t_{ELAX}	7	Address Hold Time from $\overline{ASM}$	55			ns
t_{CLAZ}	8	Address Off Time			80	ns
t_{GHDX}	9	Memory Hold Time	10			ns
t_{OZ}	10	Data Off Time from $\overline{OE}$			60	ns
t_{GLDV}	11	Memory $\overline{OE}$ Access Time			150	ns
t_{QVWL}	12	Data Setup Time (Write Cycle)	30			ns
t_{WHQX}	13	Data Hold Time (Write Cycle)	30			ns
t_{WLWH}	14	$\overline{WE}$ Pulse Width	110			ns

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Figure 1 : Test Load

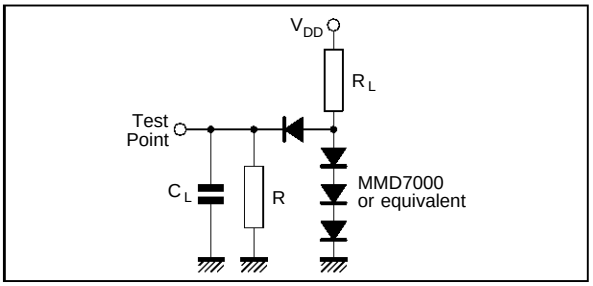

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Table 1

Symbol	AM(8:13) ADM(0:7) AD(0:7)	Other Outputs
C	100pF	50pF
R_L	1kΩ	3.3kΩ
R	4.7kΩ	4.7kΩ

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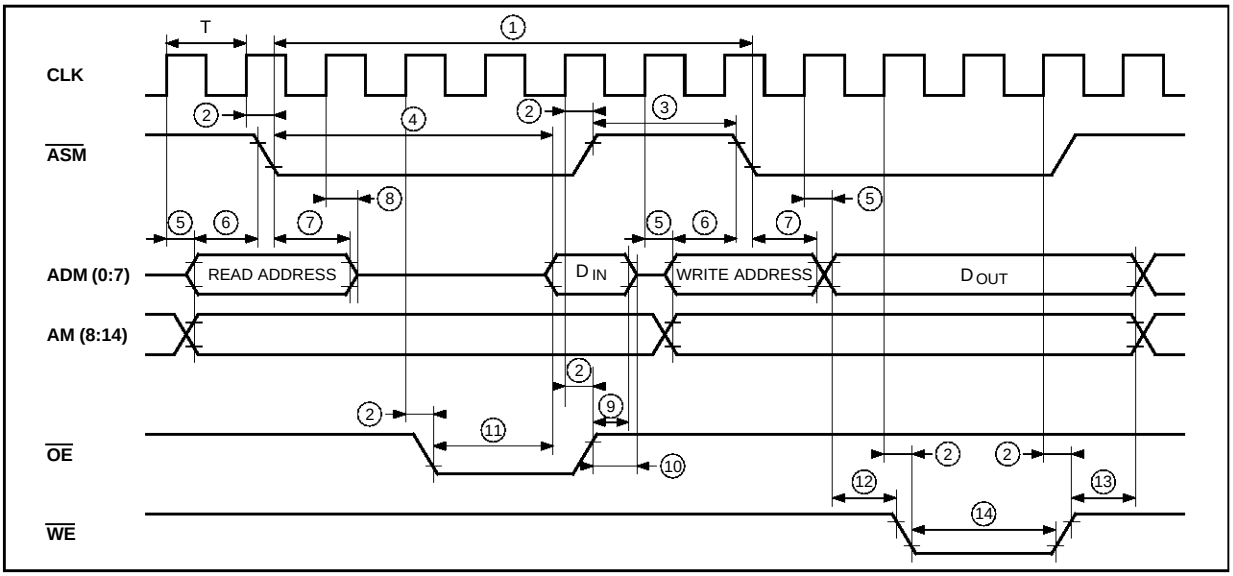
Figure 2 : Memory Interface Timing Diagram



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MICROPROCESSOR INTERFACE

EF9345 is motel compatible. It automatically selects the processor type by using AS input latch to state of the DS input.

No external logic is needed to adapt bus control signals from most of the common multiplexed bus microprocessors.

EF9345	6801	INTEL Family
	Timing 1	Timing 2
AS	AS	ALE
DS	DS, E, ϕ 2	$\overline{RD}$
R/$\overline{W}$	R/$\overline{W}$	$\overline{WR}$

MICROPROCESSOR INTERFACE TIMING AD(0:7), AS, DS, R/$\overline{W}$, CS

V_{CC} = 5.0V ±5%, T_A = 0 to + 70°C, C_L = 100pF on AD(0:7)

Reference Levels : V_{IL} = 0.8V and V_{IH} = 2V on All Inputs ; V_{OL} = 0.4V and V_{OH} on all Outputs.

Symbol	Ident. N°	Parameter	Min.	Typ.	Max.	Unit
t_{CYC}	1	Memory Cycle Time	400			ns
t_{ASD}	2	DS Low to AS High (Timing 1) DS High or R/W High to AS High (Timing 2)	30			ns
t_{ASED}	3	AS Low to High (Timing 1) AS Low to DS Low or R/W Low (Timing 2)	30			ns
t_{PWEH}	4	Write Pulse Width	200			ns
t_{PWASH}	5	AS Pulse Width	100			ns
t_{RWS}	6	R/$\overline{W}$ to DS Setup Time (Timing 1)	100			ns
t_{RWH}	7	R/$\overline{W}$ to DS Hold Time (Timing 1)	10			ns
t_{ASL}	8	Address and $\overline{CS}$ Setup Time	20			ns
t_{AHL}	9	Address and $\overline{CS}$ Hold Time	20			ns
t_{DSW}	10	Data Setup Time (Write Cycle)	100			ns
t_{DHW}	11	Data Hold Time (Write Cycle)	10			ns
t_{DDR}	12	Data Access Time from DS (Read Cycle)			150	ns
t_{DHR}	13	DS Inactive to High Impedance State Time (Read Cycle)	10		80	ns
t_{ACC}	14	Address to Data Valid Access Time			300	ns

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Figure 3 : Microprocessor Interface Timing Diagram 1 (6801 Type)

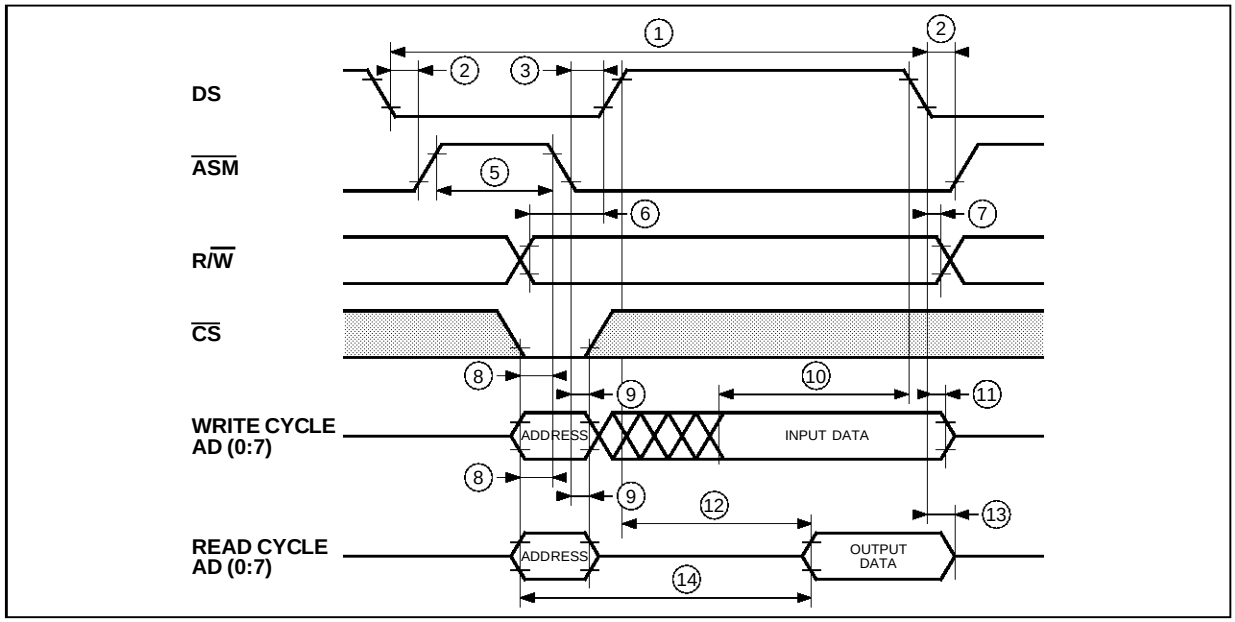

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Figure 4 : Microprocessor Interface Timing Diagram 2 (INTEL Type) - Read Cycle

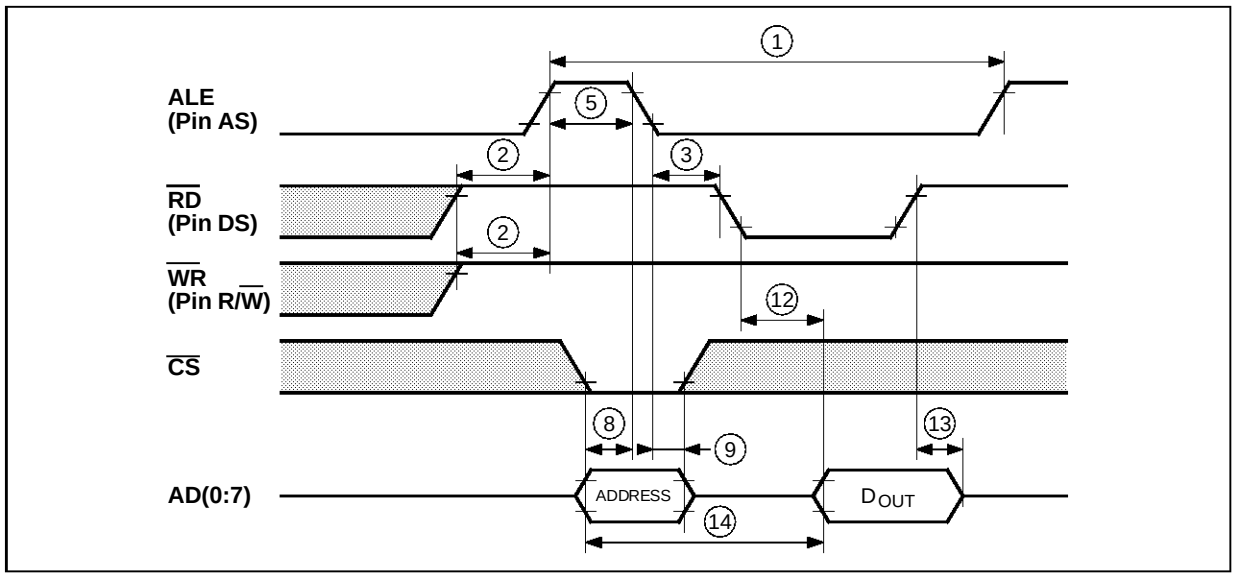
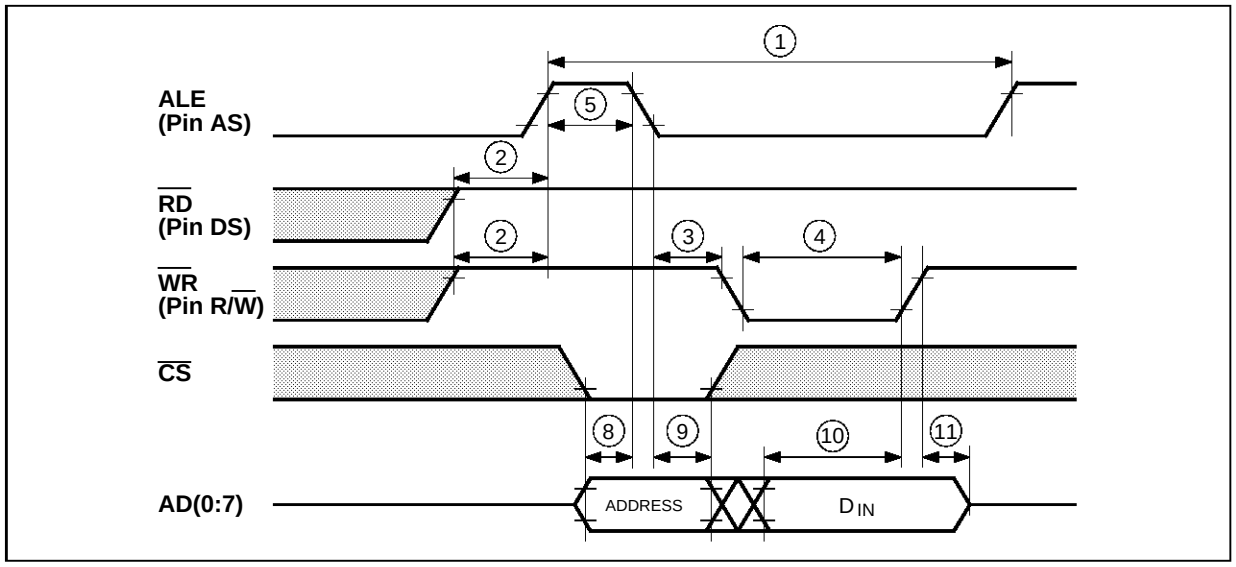


Figure 5 : Microprocessor Interface Timing Diagram 2 (INTEL Type) - Write Cycle



VIDEO INTERFACE R, G, B, I, HP, HVS/HS, PC/VS

V_{CC} = 5.0V ±5%, T_A = 0 to + 70°C, CLK Duty Cycle = 50%, C_L = 50pF
Reference Levels : V_{IL} = 0.8V and V_{IH} = 2.2V on CLK Inputs. V_{OL} = 0.4V and V_{OH} = 2.4V on all Outputs.

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SU}	Setup Time R, G, B, I to HP	10			ns
t_{HO}	Hold Time R, G, B, I from HP	50			ns
t_D	Output Delay from CLK Edge			60	ns
t_{PWCH}	CLK High Pulse Width	30			ns
t_{PWCL}	CLK Low Pulse Width	30			ns

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Figure 6

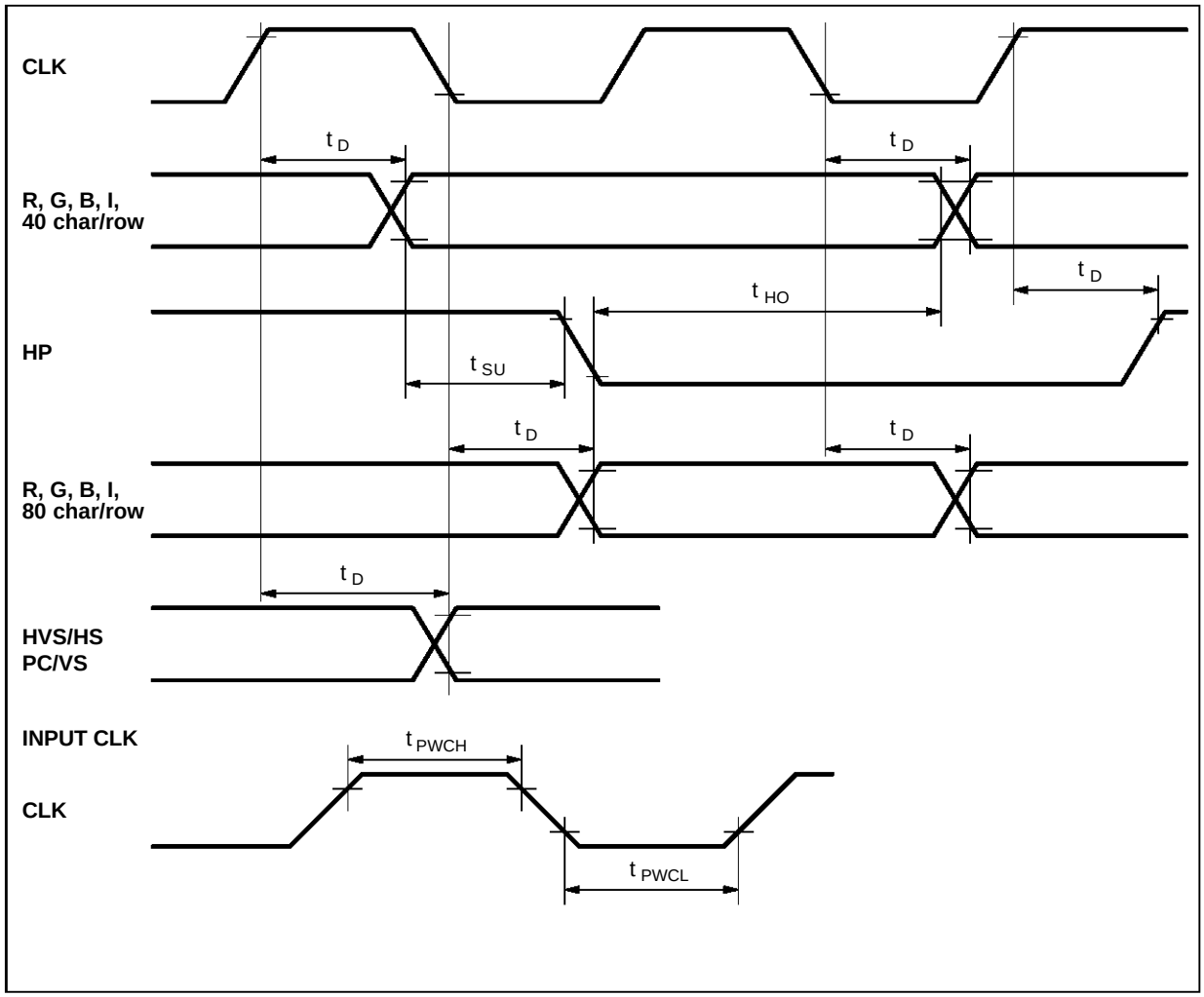

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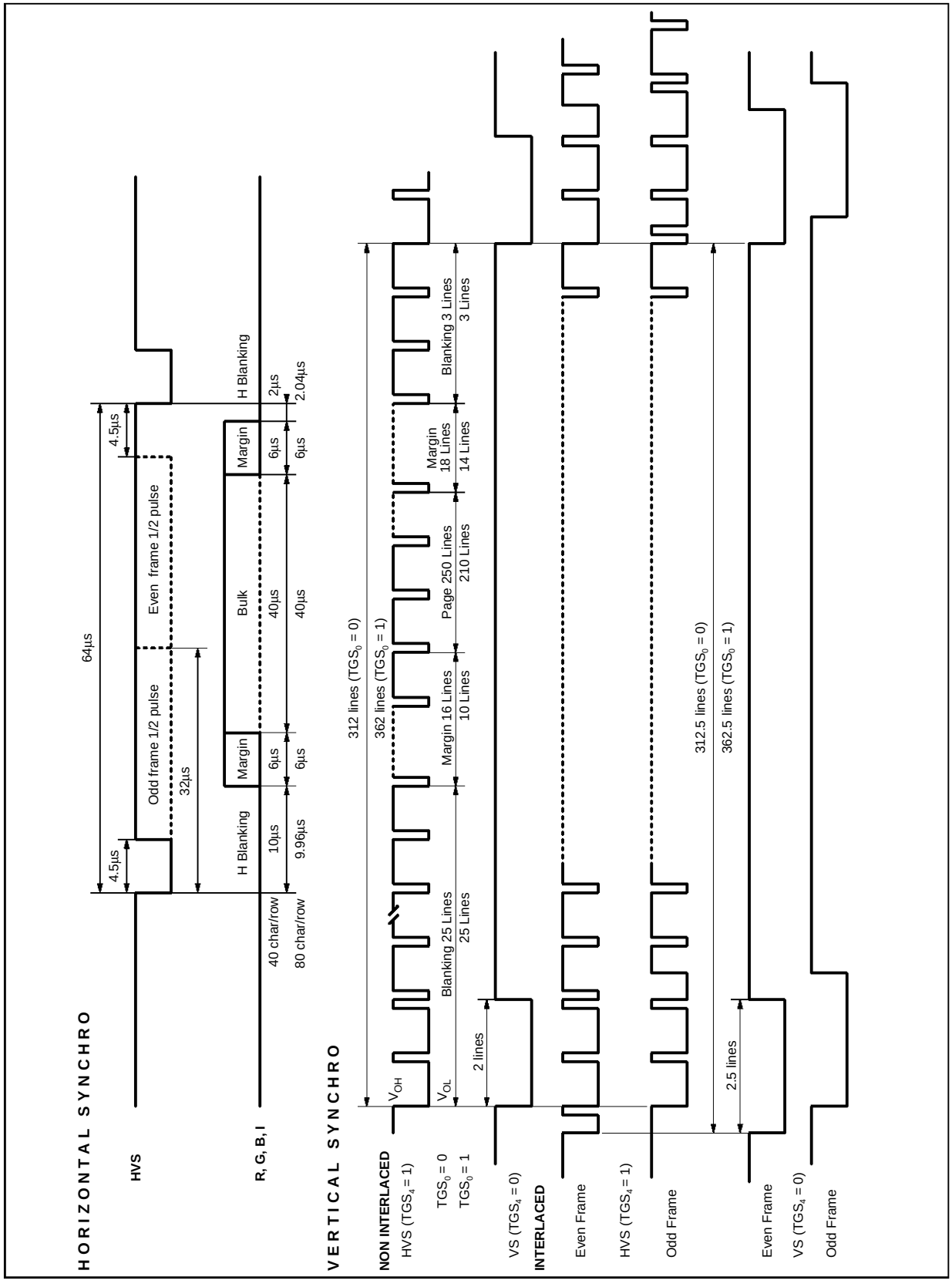
Figure 7 : Vertical and Horizontal Synchronization Outputs (CLK = 12MHz)



FUNCTIONAL DESCRIPTION

The EF9345 is a low cost, semigraphic, CRT controller.
It is optimized for use with a low cost, monochrome or color TV type CRT (64ms per line, 50 or 60Hz refresh frequency).

The EF9345 displays up to 25 rows of 40 characters or 25 rows of 80 characters.

The on-chip character generator provides a 128 standard, 5 x 7, character set and standard semigraphic sets.

More use definable (8 x 10) alphanumeric or semigraphic sets may be mapped in the 16 K x 8 private memory addressing space.

These user definable sets are available only in 40 characters per row format.

Microprocessor Interface

The EF9345 provides an 8-bit, adress/data multiplexed microprocessor interface.

It is directly compatible with popular (6801, 8048, 8051, 8035, ...) microprocessors.

Registers

The microprocessor directly accesses 8 registers :
- R0 : Command/status register.
- R1, R2, R3 : Data registers.
- R4, R5, R6, R7 : Each of these register pairs points into the private memory.

Through these registers, the microprocessor indirectly accesses the private memory and 5 more registers :
- ROR, DOR : Base address of displayed page memory and used external character generators.
- PAT, MAT, TGS : Used to select the page attributes and format, and to program the timing generator option.

Private Memory

The user may partition the 16 K x 8 private memory addressing space between :
- Page of character codes (2 K x 8 or 3 K x 8),
- External character generators,
- General purpose user area.

Many types of memory components are suitable :
- ROM, DRAM or SRAM,
- 2 K x 8, 8 K x 8, 16 K x 4 organizations,
- Modest 500ns cycle time and 250ns access time is required.

40 Characters per Row : Character Code Formats and Attributes

Once the 40 characters per row format has been selected, one character code format out of three must be chosen :
- 24-bit fixed format :
  All the attributes are provided in parallel.
- 8/24-bit compressed format :
  All the attributes are latched.
- 16-bit fixed format :
  Some parallel attributes, other are latched.

Character attributes provided :
- Background and foreground color (3 bits each),
- Double height, double width,
- Blinking,
- Reverse,
- Underlining,
- Conceal,
- Insert,
- Accentuation of lower case characters,
- 3 x 100 user definable character generator in memory,
- 8 x 100 semi-graphic quadrichrome characters.

80 Characters per Row Format : Character Code Format and Attributes

Two character code formats are provided :
- Long (12 bits) with 4 parallel attributes :
  - Blinking,
  - Underlining,
  - Reverse,
  - Color select.
- Short (8 bits) : no attributes.

Timing Generator

The whole timing is derived from a 12MHz main clock input.

The RGB outputs are shifted at 8MHz for the 40 character/row format and at 12MHz for the 80 character/row.

Besides, the user may select :
- 50Hz or 60Hz vertical sync. frequency,
- Interlaced or not,
- Separated or composite vertical and horizontal sync. ouputs.

Furthermore, a composite sync. input allows, when it is required :
- An on-chip vertical resynchronization,
- An on-chip crude horizontal resynchronization,
- An off-chip high performance horizontal resynchronization by use of a simple external VCXO controlled by the on-chip phase comparator.

MEMORY ORGANIZATION

Logical And Physical Addressing

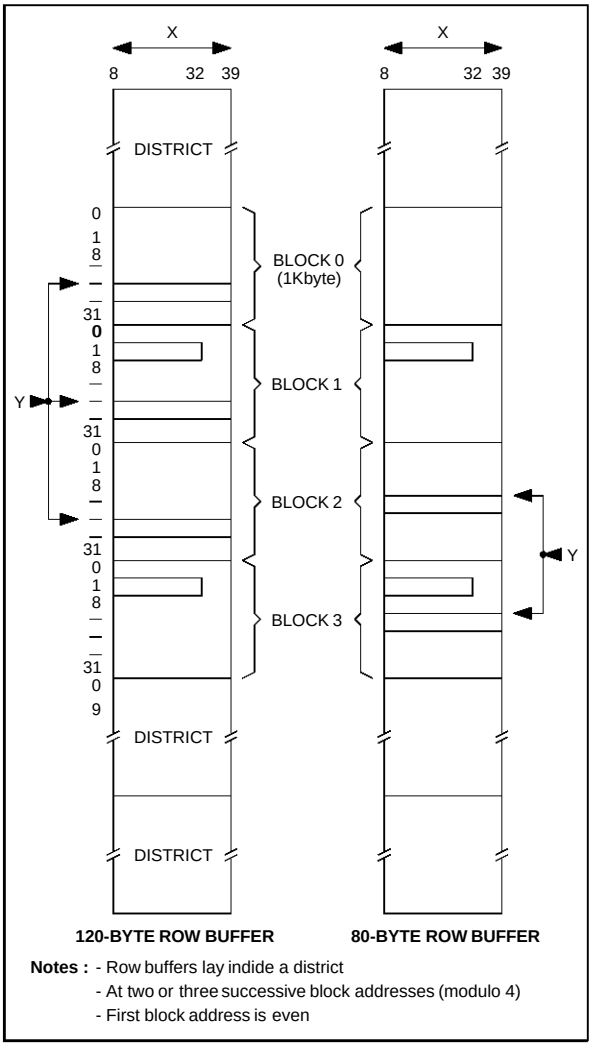
The physical 16-Kbyte addressing space is logicaly partitioned by EF9345 into 40-byte **buffers** (Figure 8). More precisely, a logical address is given by an X, Y, Z triplet where :

- X = (0 to 39) points to a byte inside a buffer,
- Y = (0, 1 ; 8 to 31) points to a buffer inside a 1 Kbyte blocks,
- Z = (0 to 15) points to a **block**.

Obviously, 1 K = 2^{10} = 1024 cannot be exactly divided by 40. Consequently, any block holds 25 full buffers and a 24-byte remainder. Provided that the physical memory is a multiple of 2 Kbytes, the remainders are paired in such a way as to make available :

- A full buffer (Y = 1) in each even block,
- A partial buffer (Y = 1 ; X = 32 to 39) in each odd block.

Figure 8 : Memory Row Buffer



Pointers

Each X, Y and Z component of a logical address is binary encoded and packed in two 8-bits registers.

Such a register pair is a pointer (Figure 9). EF9345 contains two pointers :

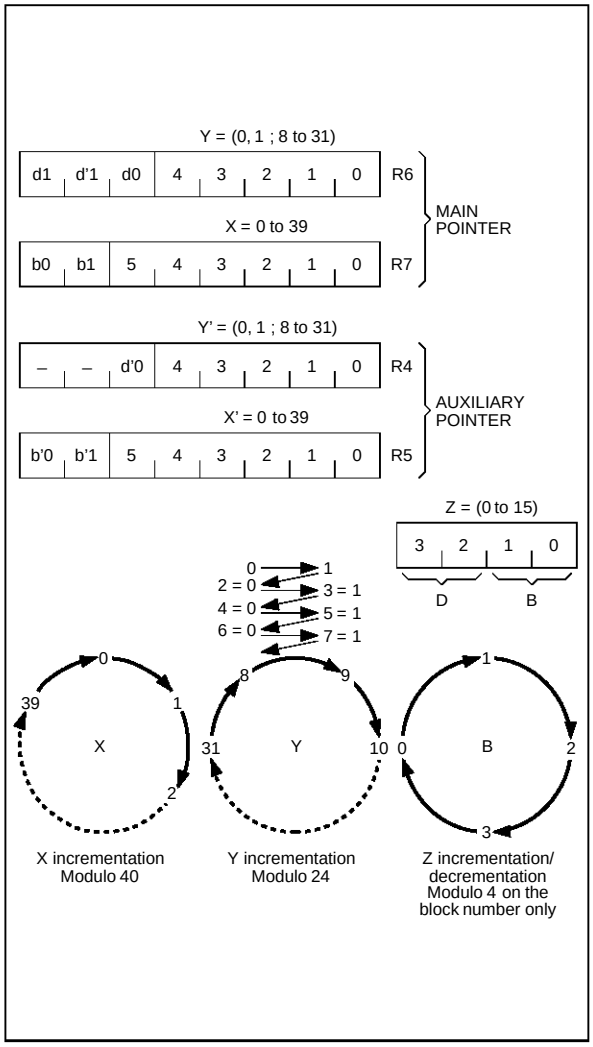
- R4, R5 : **auxiliary pointer**,
- R6, R7 : **main pointer**.

R5 and R7 have the same format. Each one holds an X component and the two LSB's of a Z component. This packing induces a partitioning of Z in 4 **districts** of 4 blocks each.

R5, R7 points to a block number in a district. R4 and R6 have a slightly different format : Each one holds a Y component and the LSB of the district number. But R6 holds both district MSB

Figure 11 gives the logical to physical address transcoding scheme performed on chip.

Figure 9 : Pointer Auto Incrementation



Data Structure in Memory

A **page** is a data structure displayable on the screen up to 25 rows of characters. According to the character code format, each row on the screen is associated with 2 (or 3) 40-byte buffers. This set of 2 (or 3) buffers constitutes a row **buffer** (Figure 8). The **buffers** belonging to a row buffer must meet the following requirements :

- They have the same Y address,
- They have the same district number,
- They lie at 2 (or 3) successive (modulo 4) block addresses in their common district.

Consequently, a row buffer is defined by its first buffer address and its format.

A page is a set of successive row buffers :

- With the same format,
- With the same district number,
- With the same block address of first buffer. This block address must be even,
- Lying at successive (modulo 24) Y addresses.

Consequently, a page should not cross a district boundary. General purpose memory area may be used but should respect the buffer of row buffer structure. See Figure 9 for pointer incrementation implied by these data structures.

Memory Time Sharing (See Figure 10)

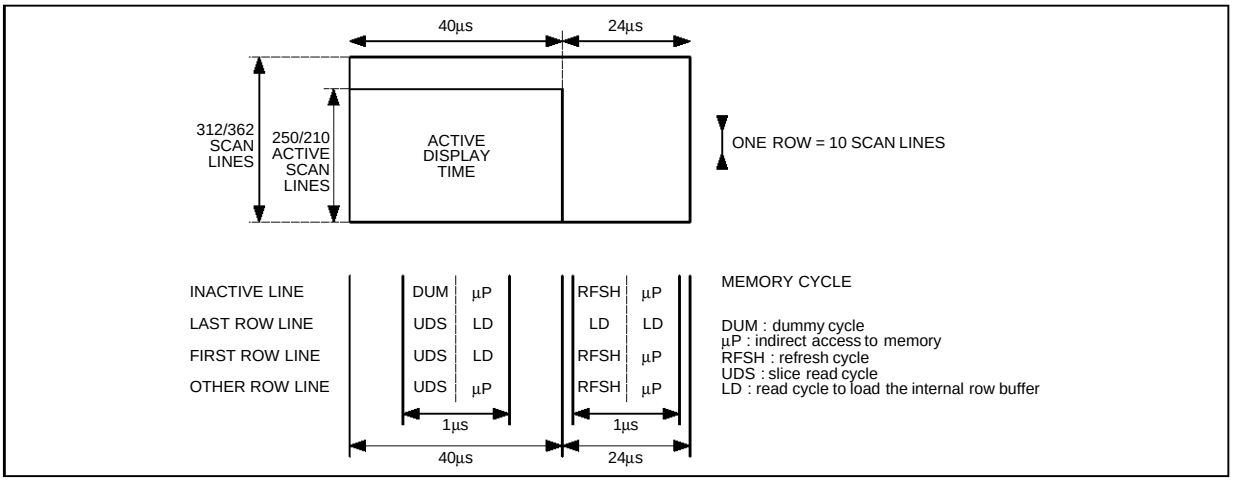
The memory interface provides a 500 ns cycle time. That is to say a 2 Mbyte/s memory bandwith. This bandwith is shared between :

- Reading a row buffer from memory to load the internal row buffer (up to 120 bytes once each row),
- Reading user defined characters slices from memory (1 byte each µs),
- Indirect microprocessor read or write operation,
- Refresh cycles to allow DRAM use, with no overhead.

A fixed allocation scheme implements the sharing.

During these lines, no microprocessor access is provided for 104µs ; this hold too when no user defined character slices are addressed.

Figure 10 : Memory Cycle Allocation



Notes : 1. Dummy cycles are read cycles at dummy addresses.

2. RFSH cycles are read cycles performed by an 8-bit auto-incrementing counter. Low order address byte ADM(0:7) cycles through its 256 states in less than 1ms.

3. The microprocessor may indirectly access the memory once every µs, except during the first and the last line of a row, when the internal buffer must be reloaded.

Figure 11 : Logical to Physical Address Transcoding Performed On-chip

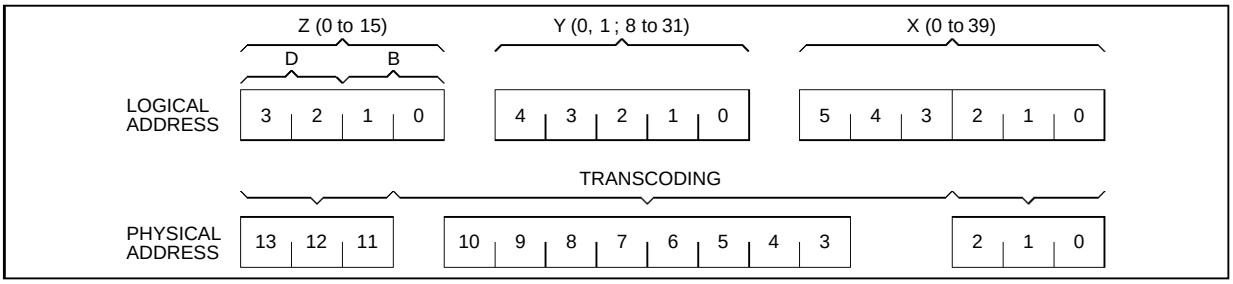


Table 2

X and Y Condition			Physical Address AM(3:10)							
			10	**9**	**8**	**7**	**6**	**5**	**4**	**3**
Y ≥ 8	X5 = 0		b0	Y4	Y3	Y2	Y1	Y0	X4	X3
	X5 = 1		b0	0	0	Y2	Y1	Y0	Y4	Y3
Y < 8	Y0 = 0		b0	0	0	X5	X4	X3	0	0
	Y0 = 1	b0 = 0	X3	0	0	I	$\overline{X5}$	$\overline{X4}$	0	0
		b0 = 1	I	0	0	I	$\overline{X5}$	$\overline{X4}$	0	0

SCREEN FORMAT AND ATTRIBUTES

The screen format and attributes are programmed through 5 indirectly accessible registers : **ROR, TGS, PAT, MAT** and **DOR**. IND command allows accessing these registers. TGS is also used to select the timing generator options (see Table 3).

Row and Character Code Format PAT$_7$; TGS$_{(6:7)}$

Two row formats and 5 character code formats are available but cannot be mixed in a given screen. DOR register interpretation is completely row format dependentand is discussed in the correspondnig 40 char/row and 80 char/row section.

Screen Partition - Page Pointer ROR

(See Table 3)

The screen is partitioned into 3 areas :
- The margin,
- The service row,
- The bulk of remaining rows.

MAT$_{(0:3)}$ declares the color of the margin and the value I_M of its insert attribute.

ROR register points to the page to be displayed and gives the 3 MSB's of the Z address : Z_0 = 0 implicitly ; the page block address must be even. YOR gives the first row buffers to be displayed at the top of the bulk area. The next row buffers to be displayed are fetched sequentially by incrementing the Y address (modulo 24). This address never gets out of the origin block. Incrementation of YOR by the microprocessor yields a roll up.

Service Row : TGS$_5$ - PAT$_0$

The service row is displayed for 10 TV lines on top of the screen and does not roll. Following TGS$_5$, it is fetched from the origin block at either Y = 0 or Y = 1. The Y = 1 is a partial row buffer. It can be used only with variable 40 char./row and an 8 byte attribute file. The service row may be disabled by PAT$_0$ = 0 ; it is the displayed as a margin extension.

BULK : TGS$_0$; PAT$_{(1:2)}$; MAT$_7$

It is displayed after the service row for 200 or 240 TV lines according to TGS$_0$. Each row buffer is usually displayed for 10 TV lines. However, MAT$_7$ = 1 doubles this figure. Then every character appears in double height (double height characters are quadrupled).

PAT$_1$ = 0 and/or PAT$_2$ = 0 disables respectively the upper 120 lines and/or the lower 80/120 lines of the bulk.

When disabled, the corresponding TV lines are displayed as a margin extension.

Cursor MAT$_{(4:6)}$

To be displayed with the cursor attributes, a character must be pointed by the main pointer (R6, R7) and MAT6 must be set. The cursor attributes are given by MAT$_{(4:5)}$:
- **Complementation :** the R, G and B of each pixel is logically negated.
  R, G, B $\rightarrow$ $\overline{R}$, $\overline{G}$, $\overline{B}$
- **Underline :** the underline attribute of this character is negated.
- **Flash :** the character is periodically displayed with, then without, its cursor attributes (50% / 50% ; ≈1Hz).

Flash Enable (PAT$_6$) - Conceal Enable (PAT$_3$)

Any character flashing attribute is a "don't care" when PAT$_6$ = 0. When PAT$_6$=1, a character flashes if its flashing attribute is set. It is then periodically displayed as a space (50% / 50% ; 0.5Hz).

PAT$_3$ is a "don't care" for 80 char./row formats.

When any 40 char./row format is in use :
- If PAT$_3$ = 0 the conceal attribute of any character is a don't care
- If PAT$_3$ = 1, the conceal attribute of each character is interpreted : a concealed character appears as a space on the screen.

Insert Modes : $PAT_{(4:5)}$

During retrace, margin and extended margin periods, the I output pin delivers the value of the insert margin attribute.

$I = I_M = MAT_4$

During active line period, the I output state is controlled by the Insert Mode and i, the insert attribute of each character. The I output pin may have several uses (see Figure 12) :

- As a margin/active area signal in the active area mark mode.
- As a character per character marker signal in the character mark mode.
- As a video mixing signal in the two remaining modes, provided that the EF9345 has been vertically and horizontally synchronized with an external video source : the I pin allows mixing RGB outputs (I = 1) and the external video signal (I = 0). This mixing can be achieve by switching or Oring. It may occur for the complete character window (Boxing Mode) or only for the foreground pixels (Inlay Mode).

Table 3 : Video Outputs During Active Periods

Insert Mode	Char. Level		Outputs	
	i	Pixels (1)	I	R, G, B (2)
Active Area Mark		–	1	X
Character Mark	0	–	0	X
	1	–	1	X
Boxing	0	–	0	BLACK
	1	–	1	X
Inlay	0	–	0	BLACK
	1	BACKGND	0	BLACK
		FOREGND	1	X

Notes : 1. Pixel type :
– : Dont't care.
FOREGRND = A foreground pixel is :
- Any pixel of a quadrichrome character,
- A pixel of a bichrome character generated from a "1" in the character generator cell.

2. RGB outputs :
X : Not affected.
BLACK : Forced to low level.

Timing Generator Options : TGS(0:4)

$TGS_{(0:1)}$ select the number of lines per frame :

TGS_1	TGS_0	LINES	
0	0	312	NON INTERLACED
0	1	262	
1	0	312.5	INTERLACED
1	1	262.5	

The composite incoming SYNC IN signal is separated into 2 internals signals :

- Vertical Synchronization In (VSI),
- Horizontal Synchronization In (HSI).

TGS_3 enable VSI to reset the internal line count. SYNC IN input is sampled at the beginning of the active area of each line. When the sample transits from 1 to 0, the line count is reset at the end of the current line.

TGS_2 enables HSI to control an internal digital phase lock loop. HSI and on-chip generated HS Out are considered as in phase if their leading edges match at ±1 clock period.

When they are out of phase, the line period is lengthened by 1 clock period (≈80ns).

TGS_4 controls the SYNC OUT pins configuration :

TGS4	HVS / HS	PC / VS
1	Composite Sync	PC
0	H Sync Out	V Sync Out

PC is the output of the on-chip phase comparator.

An external VCXO allows a smoother horizontal phase lock than the internal scheme.

Figure 12

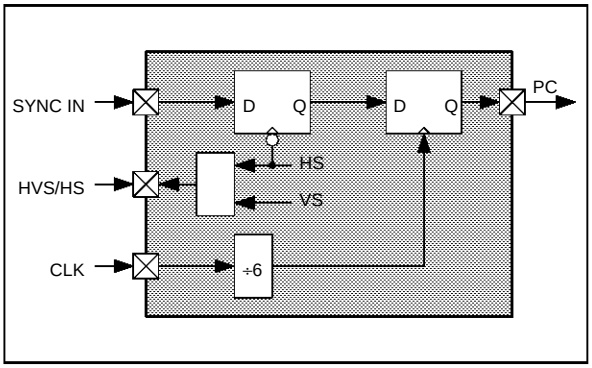
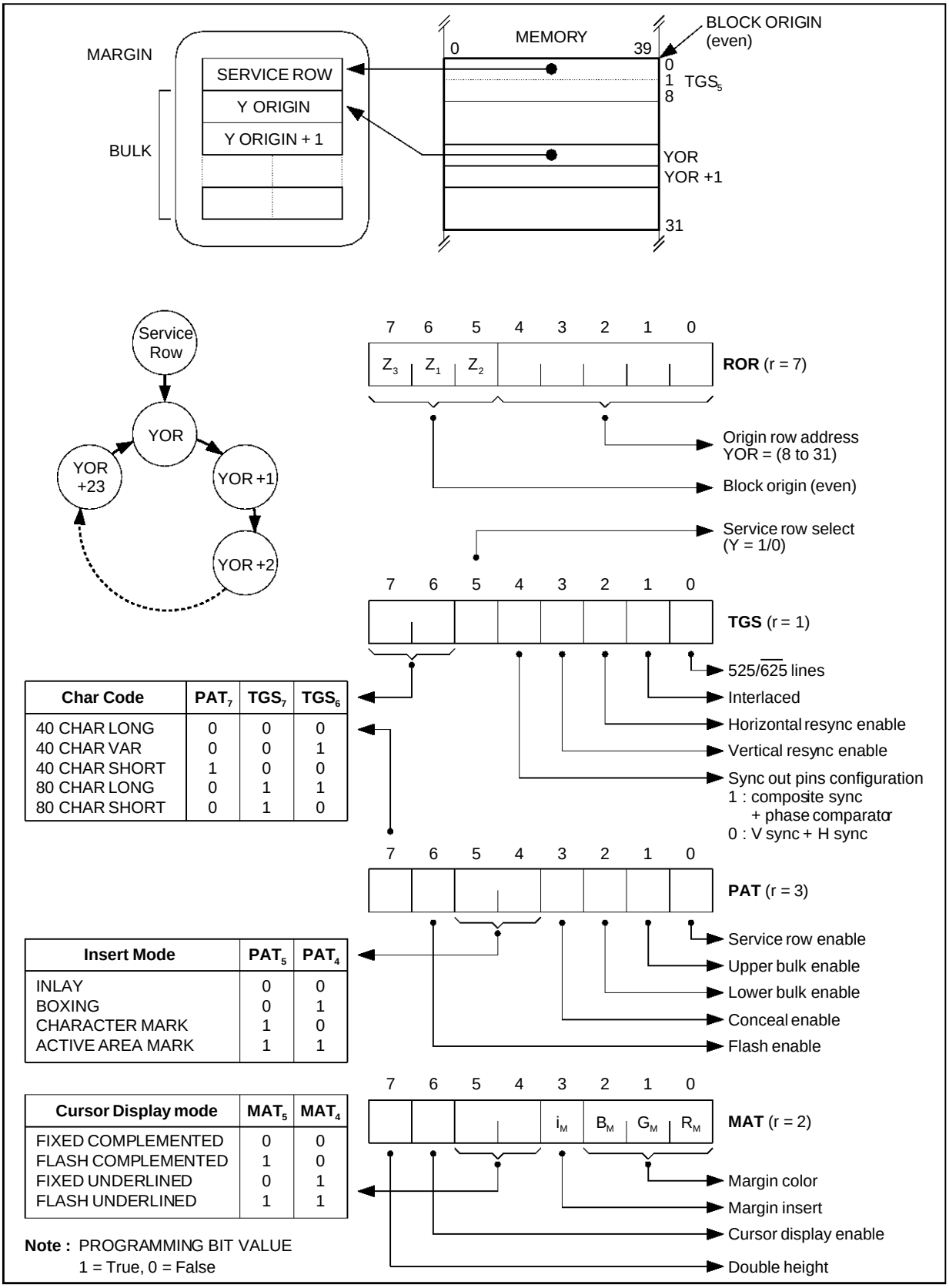


Table 3 : Screen Format



Char Code	PAT_7	TGS_7	TGS_6
40 CHAR LONG	0	0	0
40 CHAR VAR	0	0	1
40 CHAR SHORT	1	0	0
80 CHAR LONG	0	1	1
80 CHAR SHORT	0	1	0

Insert Mode	PAT_5	PAT_4
INLAY	0	0
BOXING	0	1
CHARACTER MARK	1	0
ACTIVE AREA MARK	1	1

Cursor Display mode	MAT_5	MAT_4
FIXED COMPLEMENTED	0	0
FLASH COMPLEMENTED	1	0
FIXED UNDERLINED	0	1
FLASH UNDERLINED	1	1

Note : PROGRAMMING BIT VALUE
1 = True, 0 = False

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40 CHAR/ROW CHARACTER CODES

To display pages in 40 character per row format, one out of three character code formats must be selected :

- Fixed long (24 bits) code : all parallel attributes.
- Fixed short (16 bits) code : mix of parallel and latched attributes.
- Variable (8/24 bits) code : all latched attributes.

Fixed short and variable codes are translated into fixed long codes by EF9345 during the internal row buffer loading process. The choice of the character code format is obviously a display flexibility/memory size trade off, left up to the user.

Fixed Long Codes

This is the basic 40 char./row code. Each 8 pixels x 10 lines character window, on the screen is associated with a 3-byte code in memory, namely the C, B and A bytes (Figure 13). A row on the screen is associated with a 120 byte row buffer in memory.

3-BYTE Code Structure

1. C7 is a don't care. Up to 128 characters may be addressed in each set. Each user definable set holds only 100 characters : C byte value ranges from 00 to 03 and 20 to 7F (hexa).
2. B(4:7) give the type and set number of the character.
3. All the bichrome characters have the same attributes except that alphanumerics may be underlined, semi-graphics cannot. Accentuated alphanumerics allow orthogonal accentuating of any one of the 32 lower case ROM characters with any of 8 accents (see Figure 27).
4. Bichrome and quadrichrome characters use two different coloring schemes.

For bichrome characters, character code byte A defines a two color set by giving directly two color values (Figure 14). The negative attribute exchanges the two values. Each bit of slice byte selects one color value out of two.

The "A" byte in a quadrichrome character code defines an ordered 4 color set (Figure 15). When more than 4 bits are set, higher ranking bits are ignored. When less than 4 bits are set, the color set is completed with implicit "white" value. The slice byte is shifted 2 bits at once at half the dot frequency (≈4MHz).

Each bit pair designates one color out of the 4 color sets.

Quadrichrome characters allow displaying up to 4 different colors (instead of 2) in any 8 x 10 window at the penalty of an halved horizontal resolution.

By programming the R attribute in byte B, one may chose to keep the full vertical resolution (1 slice per line) or to halve it (each slice is repeated twice). In any case, it is possible to change the color set freely from window to window and to mix freely all the character types. So, fairly complex pictures may be displayed at low memory cost.

Handling Long Codes

The KRF command allows an easy X, Y random access or an X sequential access to/from the microprocessor from/to a memory row buffer (Figure 16).

Figure 13 : 40 Char/Row Fixed Long Codes

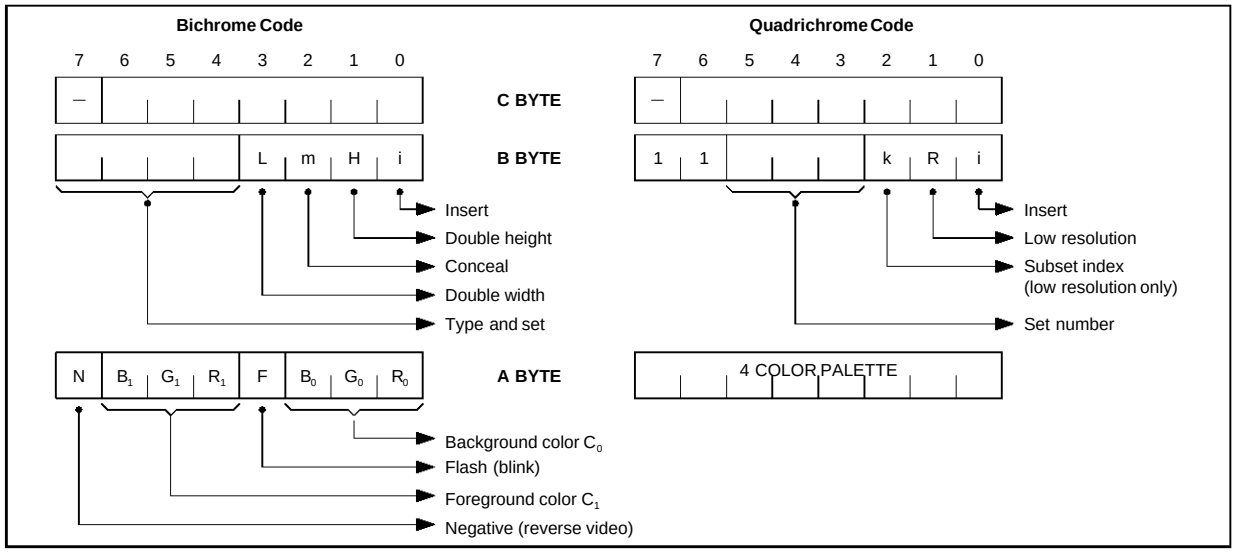

Figure 13 (Continued)

Type and Set Code : B(4:7)				Number of Character per Set	Set Name	Set Type		Cell Location
7	6	5	4	C(0:6)				
0	0	1	1	128 Standard Mosaïcs	G_{10}	SEMI-GR	BICHROME	ON-CHIP ROM
		1	0	32 Strokes	G_{11}			
	0	0	UNDERLINE	128 Alphanumerics	G_0	ALPHA		
	1	0		Accentuated Lower Case Alpha	G_{20}			
		1			G_{21}			
1	0	0		100 Alpha UDS	G'_0			EXTERNAL MEMORY
	0	1	0	100 Semi-Graphic UDS	G'_{10}	SEMI-GR.		
		1	1	100 Semi-Graphic UDS	G'_{11}			
	1	X	X	8 Sets of 100 Quadrichrome Character	Q_0 to Q_7	Quadrichrome		

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Note : Programming bit value : 1 = True ; 0 = False.

Figure 14 : Coloring with Bichrome Characters

B	G	R	Color Value
0	0	0	Black
0	0	1	Red
0	1	0	Green
0	1	1	Yellow
1	0	0	Blue
1	0	1	Magenta
1	1	0	Cyan
1	1	1	White

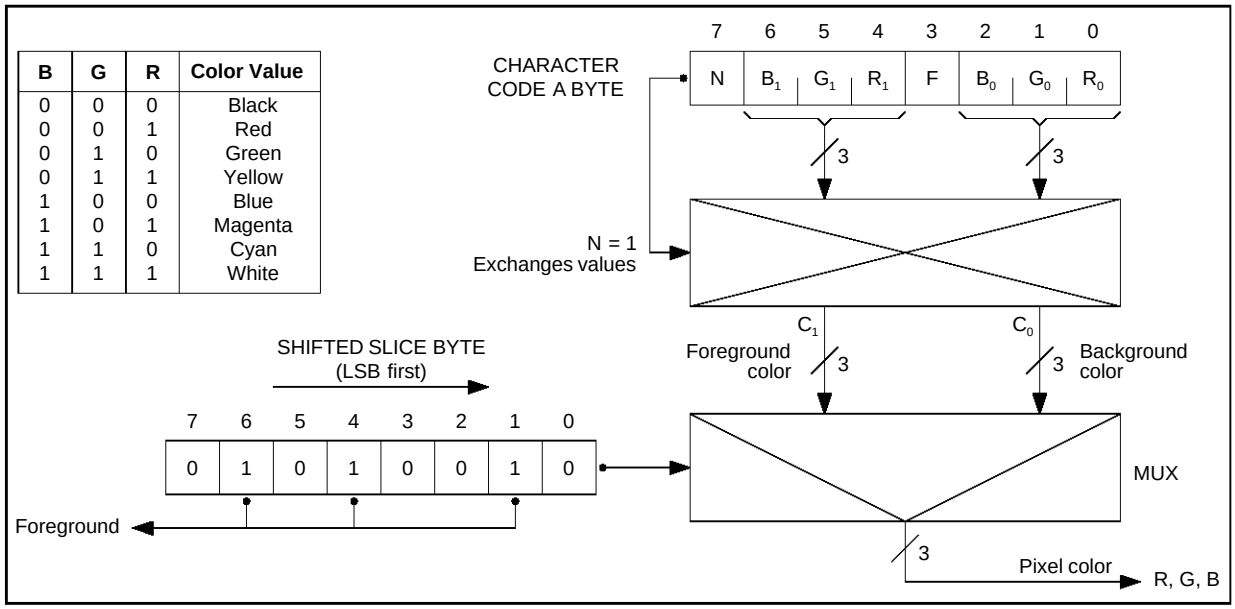

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Figure 15 : Coloring with Quadrichrome Characters

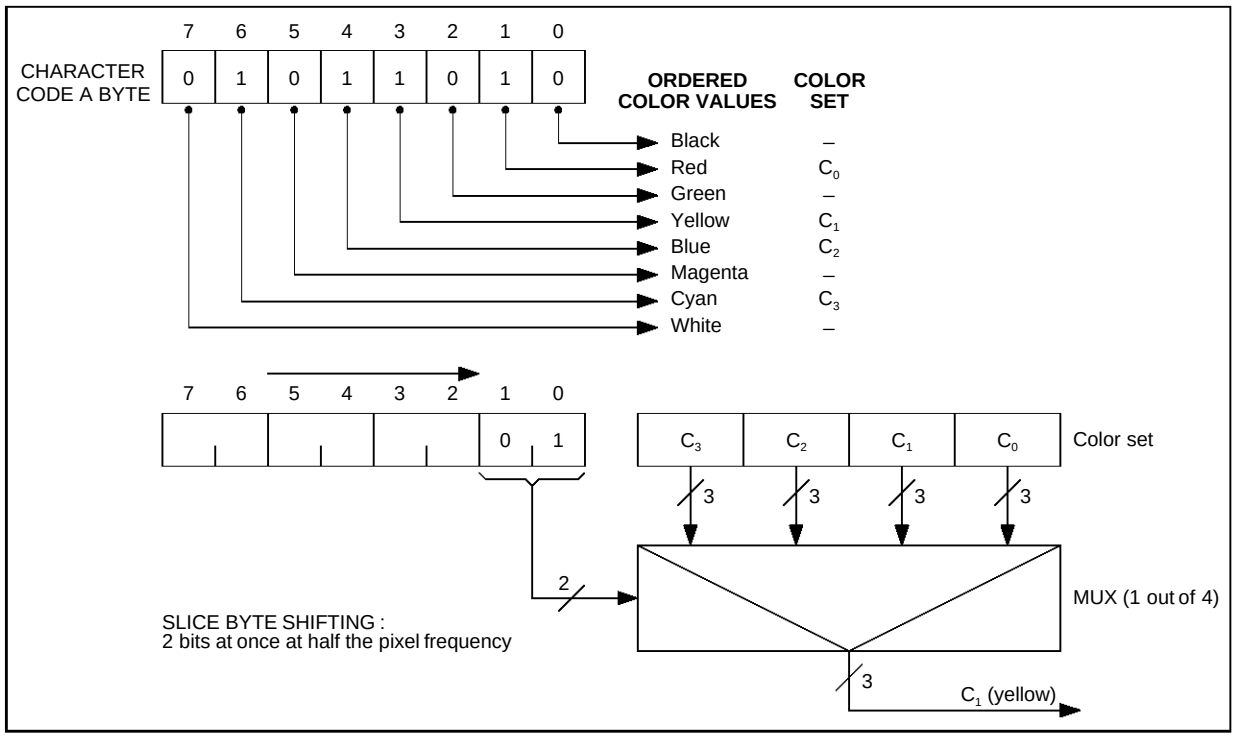
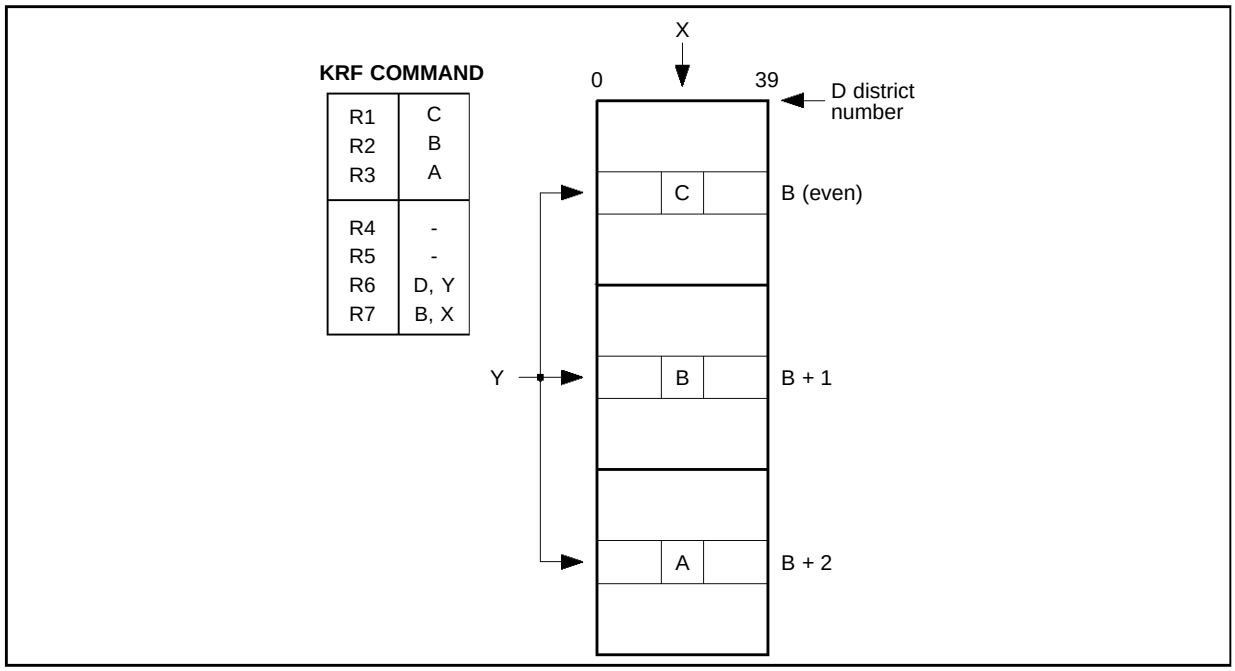


Figure 16 : Fixed Long Codes in Memory 120 Byte Row Buffer



Variable Codes

In many cases, successive characters on screen belong to the same character set and have the same attributes. Variable codes achieve memory saving by storing B and A bytes only when it is required by exploiting the C7 bit.

C7 = 1 This is a long 3-byte code.
Character set and attribute values are completely redefined by B and A bytes.

C7 = 0 This is a short 1-byte code.
Character set and attributes value are identical to the previous code.

A further saving comes from the fact that an accentuated alphabetic character is, more often than not, followed by a not accentuated alphabetic character.

So, G_{20} or G_{21} sets are processed as one-shot escape with return to G_0. For normal operation, variable codes should obey the following rules :

- The first character code of any row (X = 0) should be long.
- A character code may be short when it has the same attributes as the previous character code and belongs to the same set.

However :

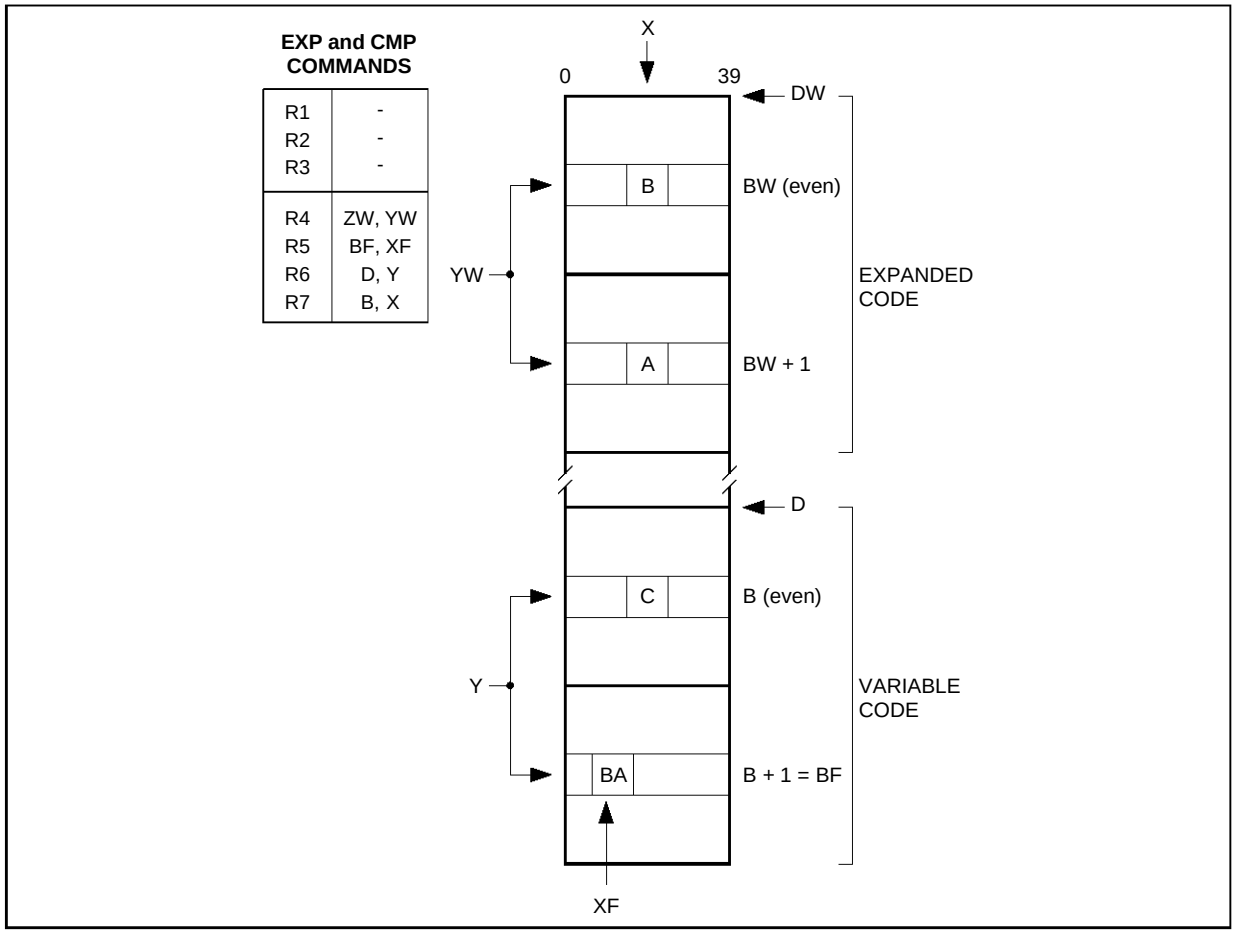
- Any code belonging to G_{20} or G_{21} must be long and must be repeated if the character is double width,
- A code belonging to G_0 following a G_{20} or G_{21} code may be short.

Handling the Variable Codes

During the display process, a row of variable code should be laid in an 80/120 byte row buffer. The first buffer holds the C bytes. The second buffer holds the B, A file providing up to 20 long codes per row (Figure 18). In the exceptional case when this is not enough, the second buffer overflows in the third one. Every code may then be long. Variable codes can almost always achieve a memory saving over long fixed codes and can never be worse.

The KRV command gives a very easy sequential access to/from a row buffer from/to the microprocessor. This command automatically updates the C byte and B, A file pointers (the last one when C7 is set).

Figure 17 : Expansion/Compression Move



Random access to a variable code is obviously not as easy. The EXP, KRE and CMP commands are designed to facilitate this task (figure 17).

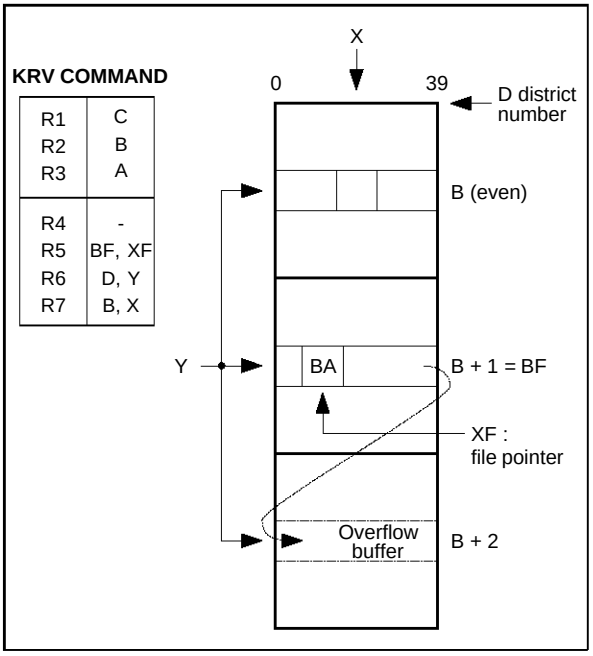
The EXP command translates a full row of variable codes into a row of expanded codes. Expanded codes are generally not displayable by very similar to the long codes.

KRE gives a random access to an expanded code and makes it appear as a regular long code.

The CMP command translates a full row of expanded code into a row of variabble codes and minimizes the file size in the process.

These commands use a buffer pair as working area.

Figure 18 : Variable Codes in memory



Fixed Short Codes

These fixed 16 bits codes achieve memory saving by another way. They may be easier to handle than variable codes. The penalty is in lesser display capabilities :

- Accentuated character sets are no longer available : accentuated characters must be individually provided by the character generators.
- G'11 and quadrichrome sets cannot be reached.
- Some attributes are latched and can be changed only while displaying a space (delimitor code).

The KRG command allows an easy access from/to an 80-byte row buffer in memory to/from the microprocessor (Figure 19). Figure 20 gives the fixed short to fixed long translation process which occurs for each row - while loading the internal row buffer before display.

Figure 19 : Fixed Short Codes in Memory 80

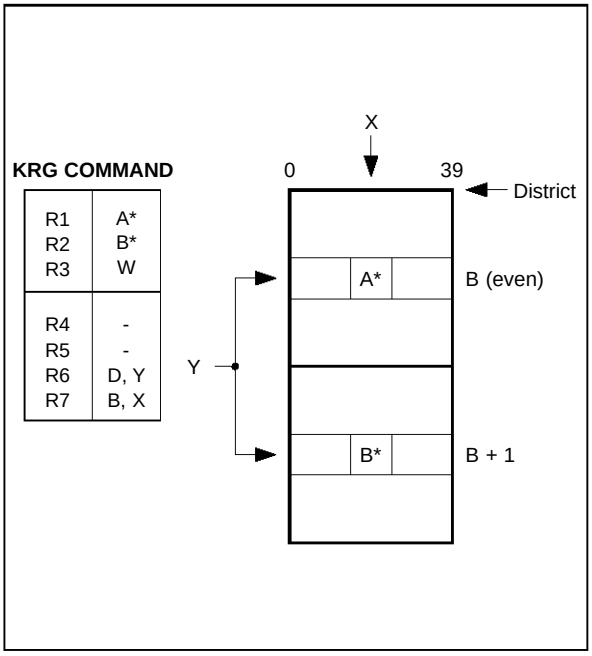
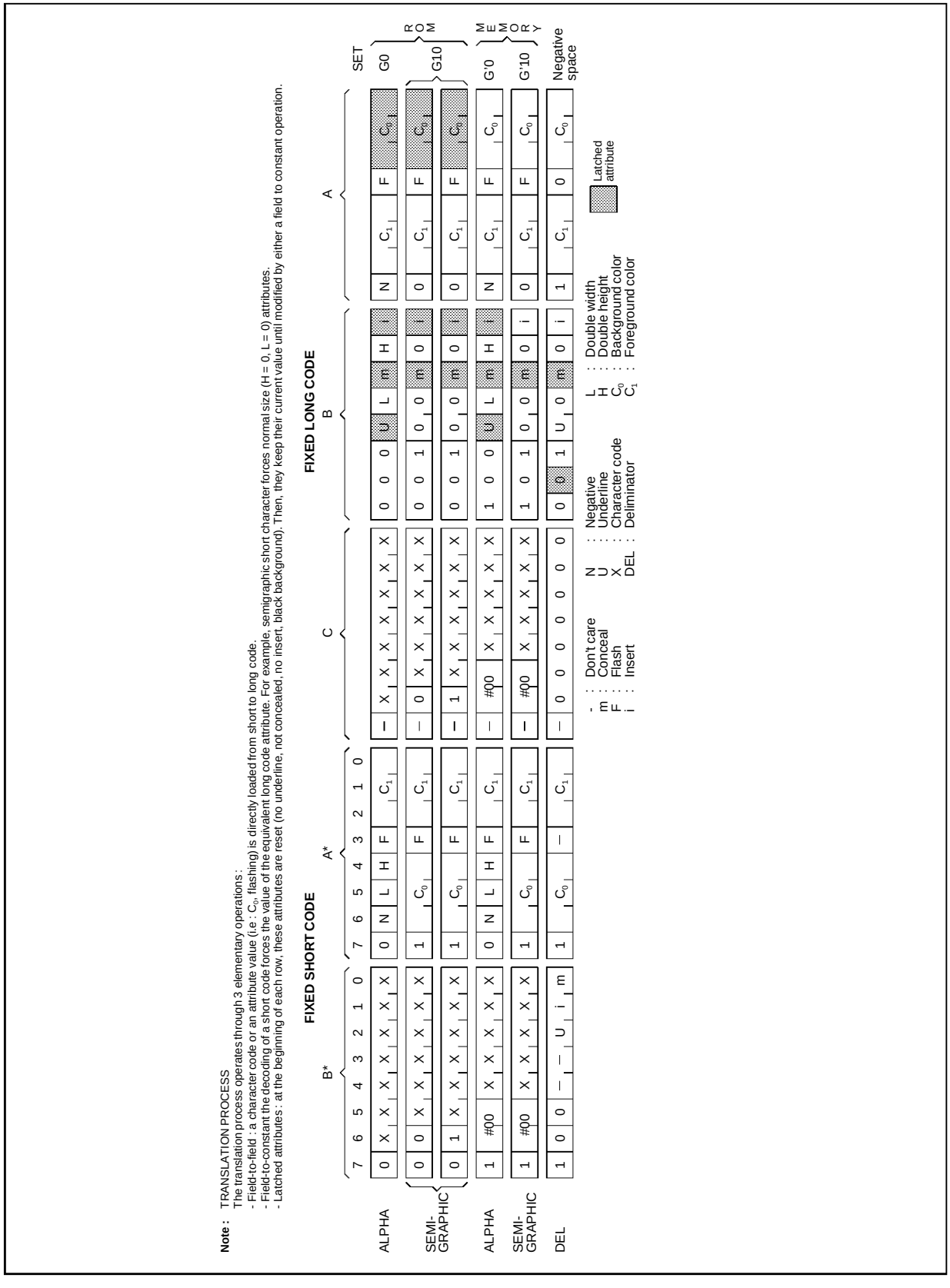


Figure 20 : Fixed Short Code to Fixed Long Code Translation



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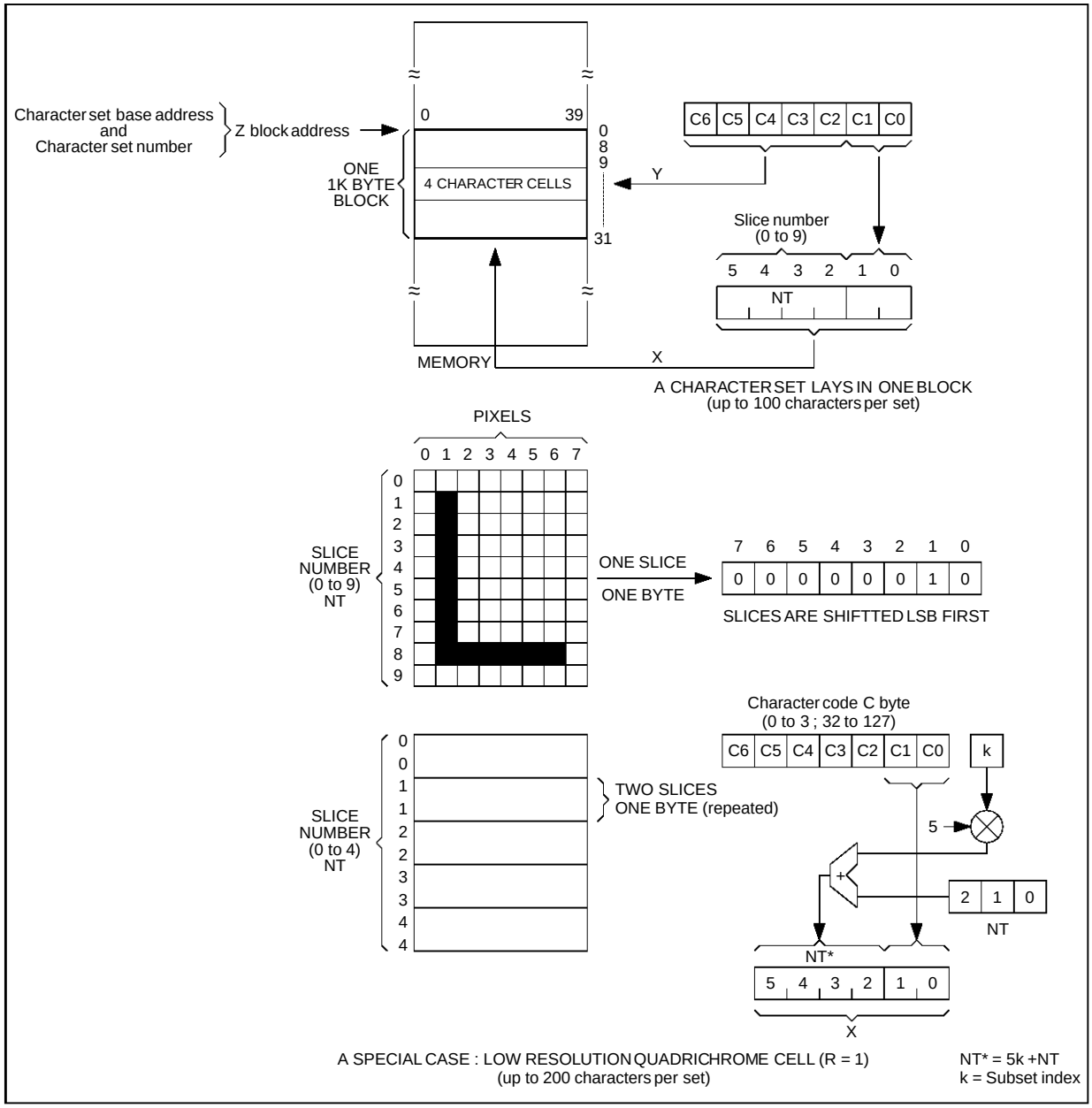
USED DEFINED CHARACTER GENERATOR IN MEMORY : DOR REGISTER

With 40 char / row, the elementary window dimensions on the screen are 10 slices x 8 pixels. Thus, a character cell holds 10 bytes in memory and 4 character cells are packed in one 40-byte buffer (Figure 21). However, 5 bytes of a low resolution quadrichrome cell are enough to fill up to window. In this case, 8 character cells can be packed in one 40-byte buffer.

Figure 21 : Packing UDS Cells in Memory



The cells of one given character set should be layed in one block.

Up to 100 character cells may be addressed in each set (or 200 for low resolution quadrichrome only). The location in memory, where to fetch the sets in use, are declared by DOR register (Figure 22). For each type of set, it gives the MSB(s) of the Z block address. EF9345 reads the Z LSB(s) in the B byte of the (equivalent) long code. As usual, the character code is read in the C byte. NT is derived from the TV line rank in the row and the double height status.

Loading User Defined Character Set

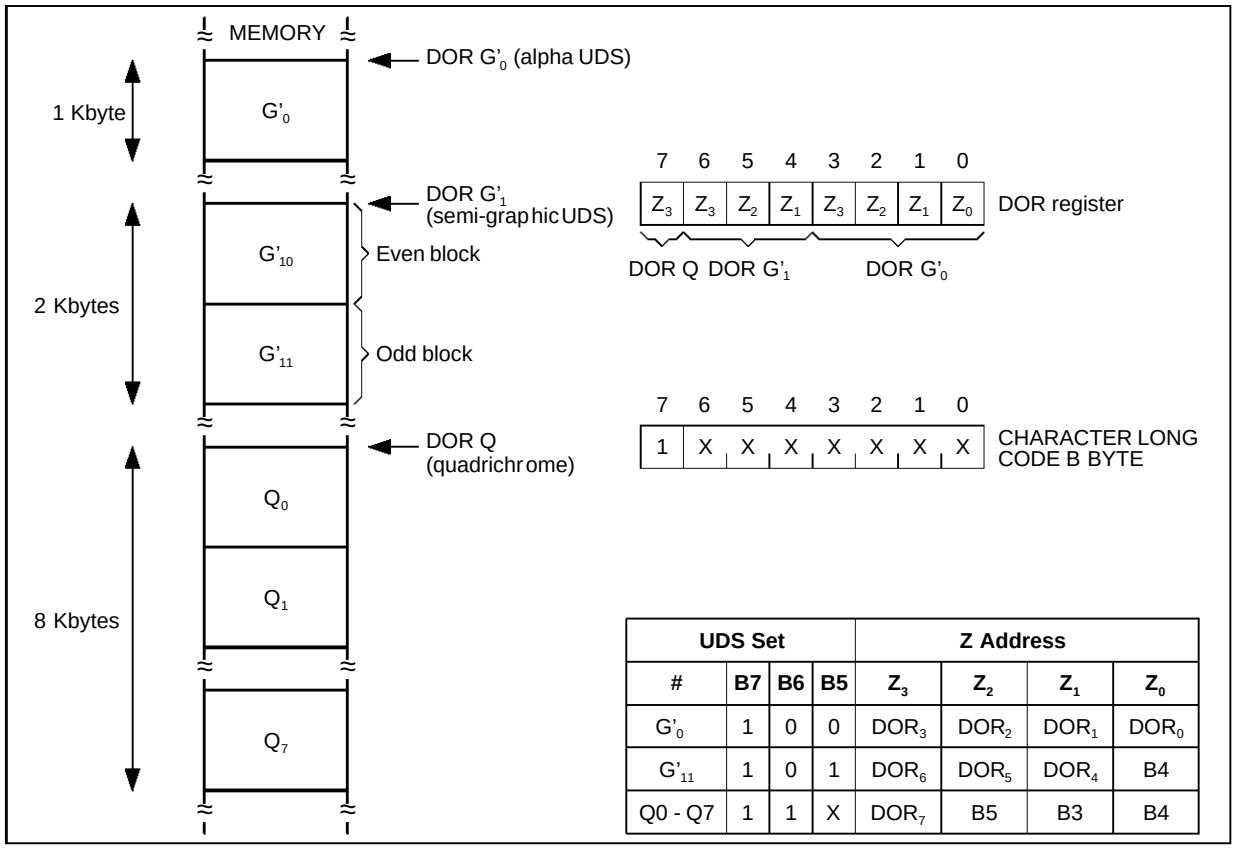
Before loading a character set into RAM, the user must :

- Assign a name to the set :
  - G'_0, G'_{10} or G'_{11} for bichrome characters.
  - From Q_0 to Q_7 for quadrichrome characters.
- Assign a character number to each character belonging to this set, character numbers range from 0 to 3 and 32 to 127.
  - It is binary coded into 7 bits C(0:6) - C(0:6) will be loaded later on into a C byte character code in order to display the character.
- A pointer to a character slice in memory is then manufactured from :
  - The character number C(0:6)
  - The slice number NT(0:3)
  - The block number assigned to the set Z(0:3)

Figure 23 shows how to proceed with the auxiliary pointer and the OCT command.

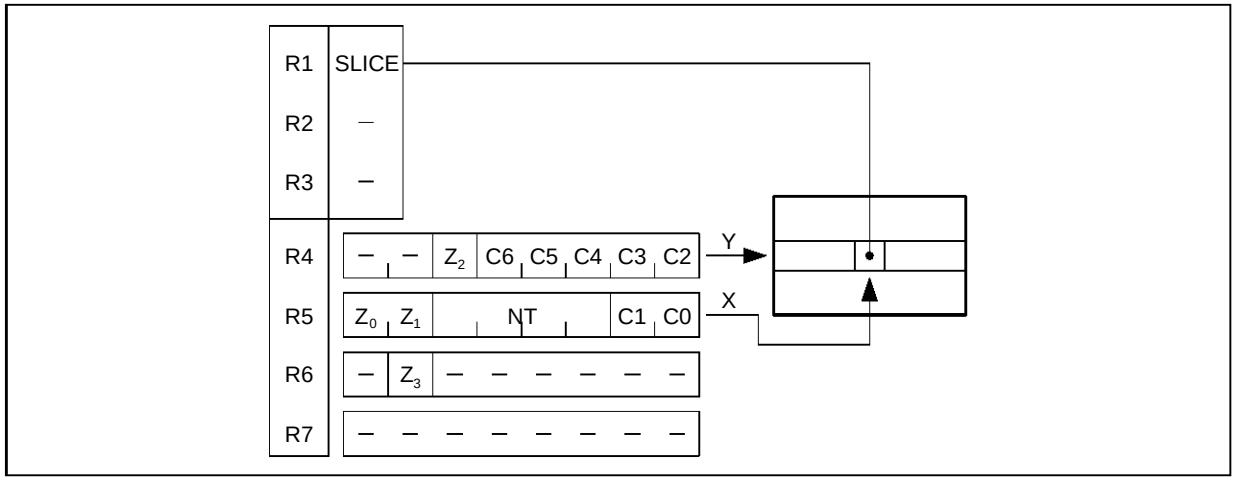
Note : The main pointer may be also used. When sequentially accessing slices of a given character, auto incrementation is helpless.

Figure 22 : UDS Fetch to Display



UDS Set				Z Address			
#	B7	B6	B5	Z_3	Z_2	Z_1	Z_0
G'_0	1	0	0	DOR_3	DOR_2	DOR_1	DOR_0
G'_{11}	1	0	1	DOR_6	DOR_5	DOR_4	B4
Q0 - Q7	1	1	X	DOR_7	B5	B3	B4

Figure 23 : Accessing a Character Slice in Memory Using OCT Command with Auxiliary Pointer



On-Chip Character Generator

- G_0 set is common to 40 and 80 char./row modes (Figure 24 and Figure 34).
- G_{10} is the standard mosaïc set for videotex (Figure 25).
- G_{11}, G_{20} and G_{21} cannot be reached from the 16-bit short fixed codes (Figure 26 and Figure 27).

Displaying the Attributes

1. For normal operation, a double height and/or double width character must be repeated in memory in two successive Y and/or X positions. The user may otherwise freely mix any character size.
2. The attributes are logically processed in the following order :
   - Underline or underline cursor : foreground forced on the last slice (NT = 9).
   - Flash : background periodically forced on the whole window (0.5Hz). The phase depends on the negative attribute.
   - Conceal : background forced permanently on the whole window. A concealed character neither blinks nor is underlined.
   - Negative : exchange the background and foreground color values when set.
   - Coloring.
   - Complemented cursor mode.
   - Insert : black color forced when required.
3. Basic pixel shift frequency : f_{CLK} x 2/3 = 8MHz.

Figure 24 : G_0 Alphanumeric Character Set in 40 Character/Row Mode

C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

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Figure 25 : G_{10} Semigraphic Character Set

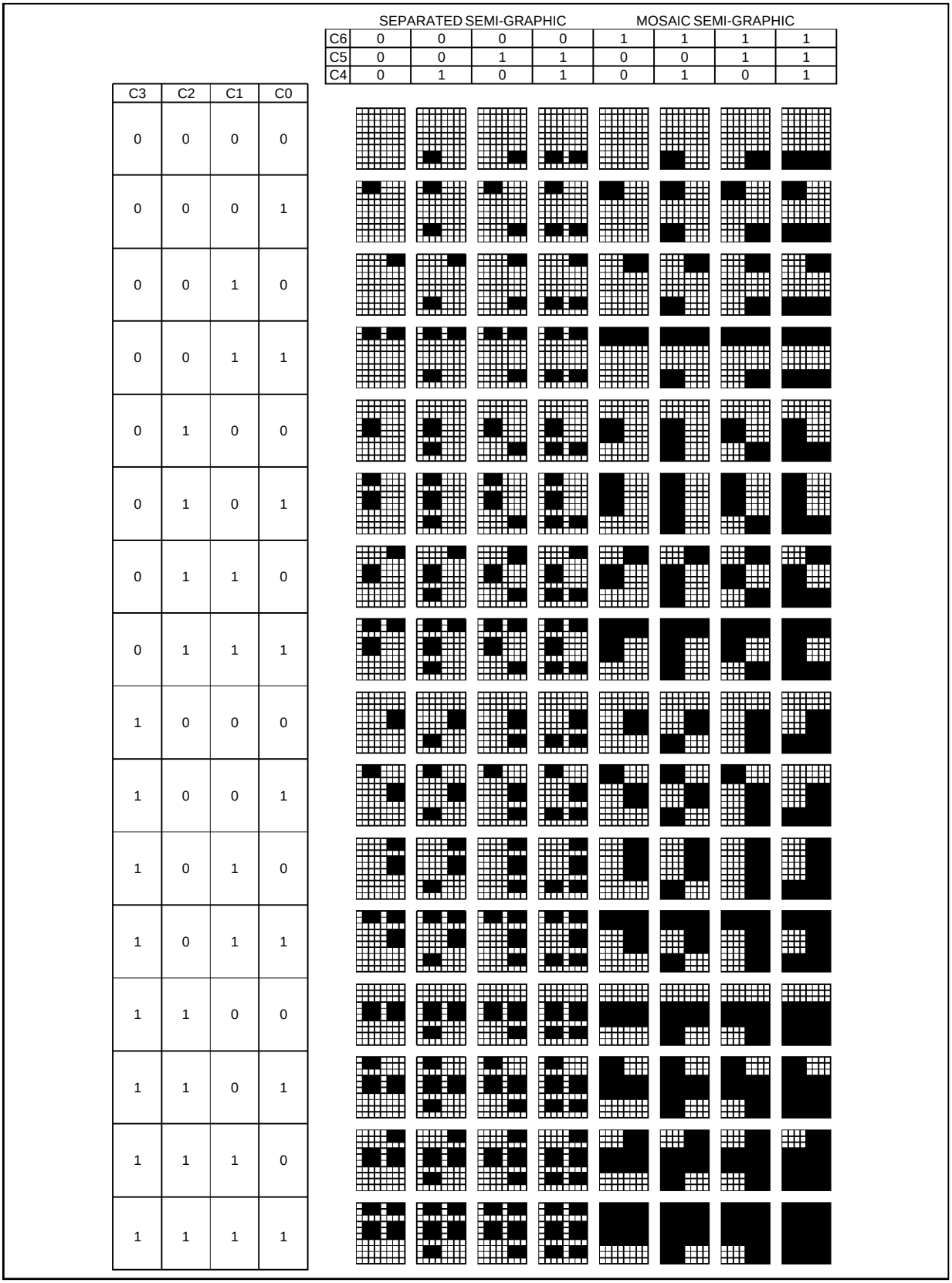

Figure 26 : G_{11} Stroke Set

C5	0	0
C4	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

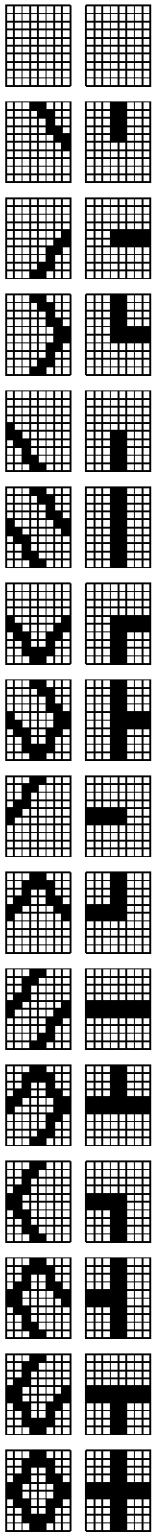

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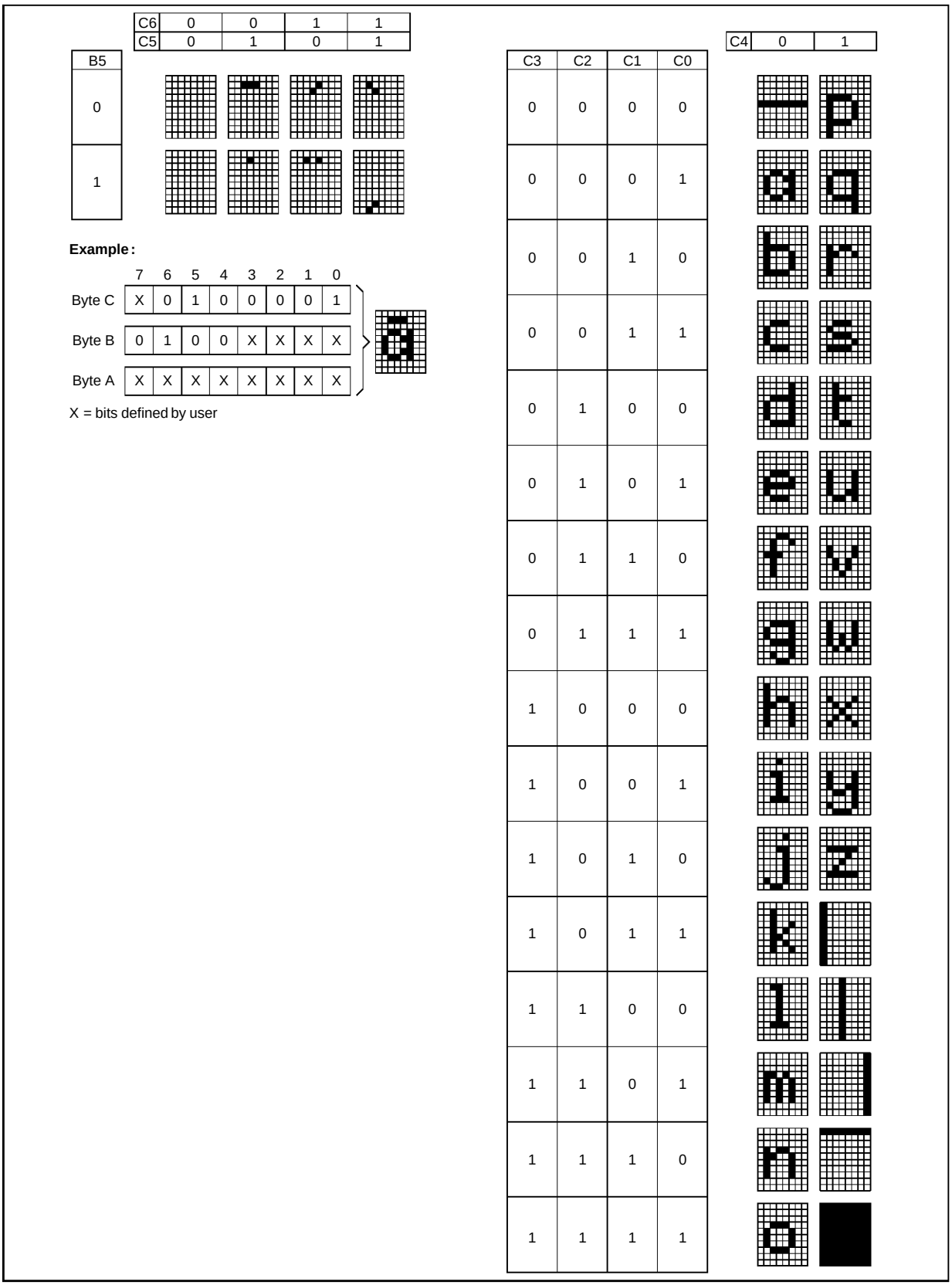
Figure 27 : G_{20} and G_{21} Accentued Character Sets



80 CHAR/ROW CHARACTER CODES

To display pages in 80 character per row format, one of two character code formats must be selected :

- Long (12 bits) code : 4 parallel attributes and large on-chip 1024 semigraphic character set,
- Short (8 bits) code : no attribute, no semigraphic set.

Both formats address the on-chip G0 set (128 characters 6 x 10). None allows UDS addressing.

Long Codes

Each 6 pixels x 10 lines character window on the screen is associated with a 12-bit code in memory, namely a C byte and an attribute nibble A (Figure 18). C7 bit designates the set.

- Alphanumeric set : C7 = 0
  C(0:6) designates one out of 128 alphanumeric characters in the G0 on-chip set. This set is common to the 40 char/row format, with the 2 right most columns truncated (see Figure 34).
  A(0:3) gives 4 parallel attributes.
- Mosaïc set : C7 = 1
  A(1:3) and C(0:6) address a dedicated mosaïc character. Each of these address bits controls the foreground/background status of a 3 pixels x 2 lines sub-window : foreground when the bit is set.

A0 provides a color select attribute.

Short Codes

They are derived from the long code by giving a 0 implicit value to each bit of the A nibble : positive, not underlined, not flashing.

Packing the Codes in Memory

Long codes are paired. A pair is packed in a 3-byte word. Therefore, the 80 codes of a row fill a 120-byte row buffer (Figure 29). The left most position on the screen is even. Its corresponding C byte is at the beginning of the first buffer. The next position on the screen is odd. Its corresponding C byte is at the beginning of the second buffer. Both nibbles are packed in the third buffer. With short codes, the same scheme yields 80-byte row buffers.

Access to the Codes in Memory

KRL command transfers 12 bits from/to the R1 and R3 registers to/from memory. The read modify write operation, necessary to write the A nibble in memory, is automatically performed provided that the A nibble is repeated in the R3 register (Figure 30). Dedicated auto-incrementation is also performed when required.

KRC command does a similar job for the short codes (Figure 31).

A very simple scheme allows the microprocessor to transcode an horizontal screen location into a pointer (Figure 32). The joint use of this scheme with the dedicated command alleviates all the packing/unpacking troubles.

Figure 28 : 80 Char/Row Character Code

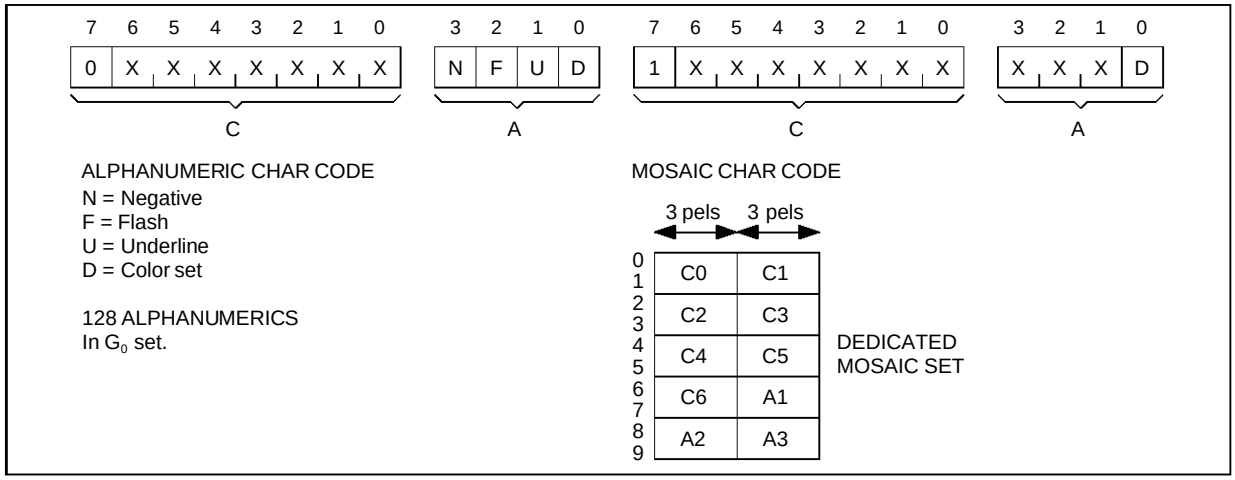


Figure 29 : 80 Char/Row Character Code Packing

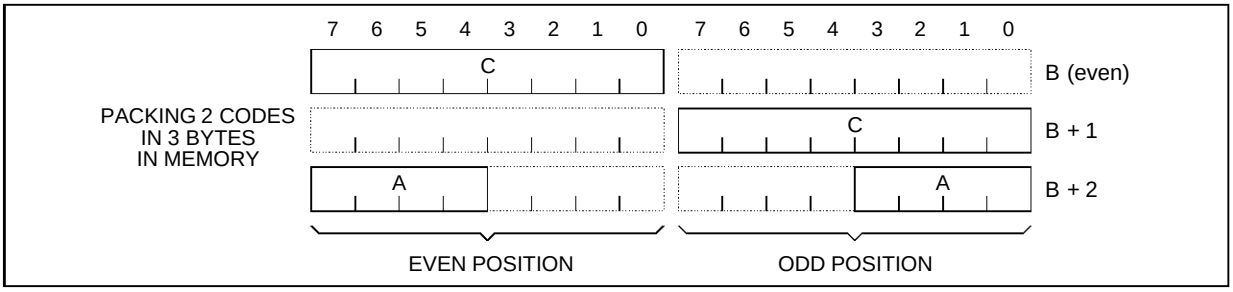
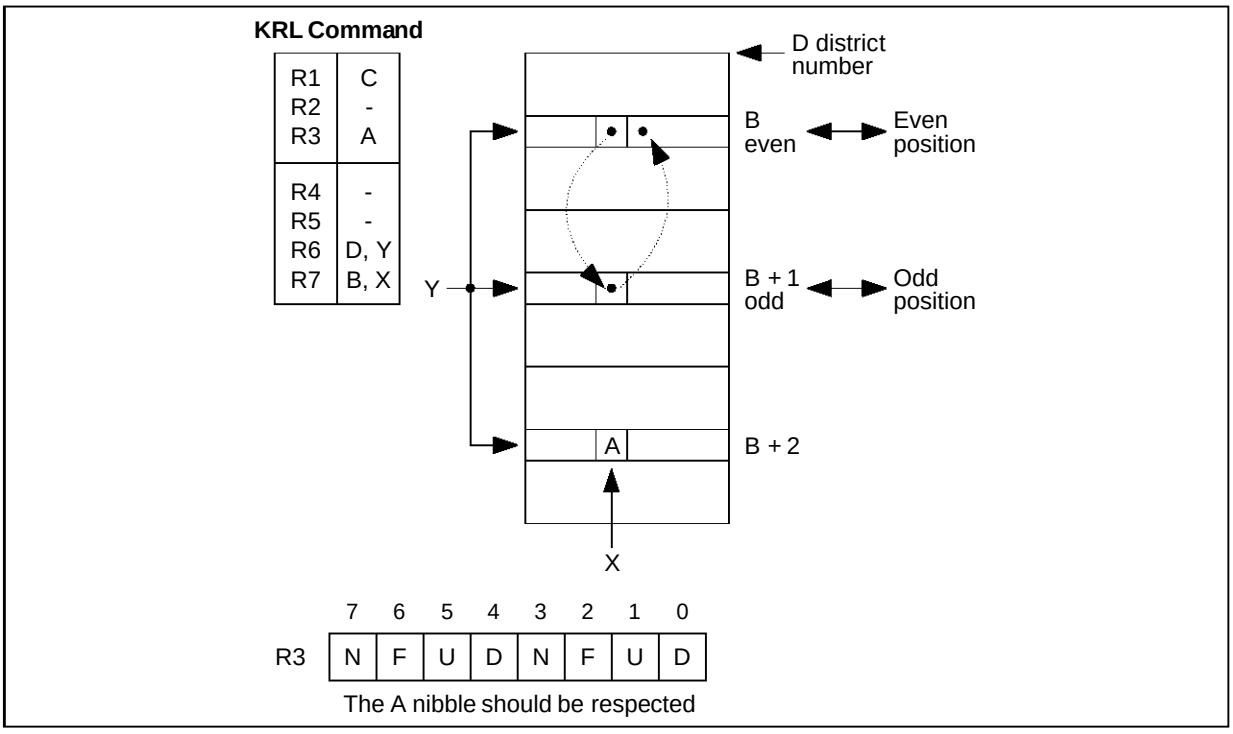


Figure 30 : KRL Command : Sequential Access to Long Codes



Displaying the Attributes - DOR Register

Short code and mosaïc characters are not flashing, not underlined and "positive".

The attributes are processed in the following order :

- Underline or underlined cursor : foreground is forced on the last slice (NT = 9).
- Flash : background is periodically (0.5Hz - 50%) forced on all the window. The phase depends on the negative attribute.
- Color select : a "positive" character is displayed with a background color same as the margin color. The foreground color is selected in DOR register by the D attribute.
- Negative : when the character is negative, background and foreground colors are exchanged. In complemented CURSOR position, these colors are complemented.
- Insert : the D attribute selects one insert value in DOR register. This attribute is then processed up to the current insertion mode (see screen format and attribute insert section.

Figure 31 : KRC Command : Sequential Access to Short Codes

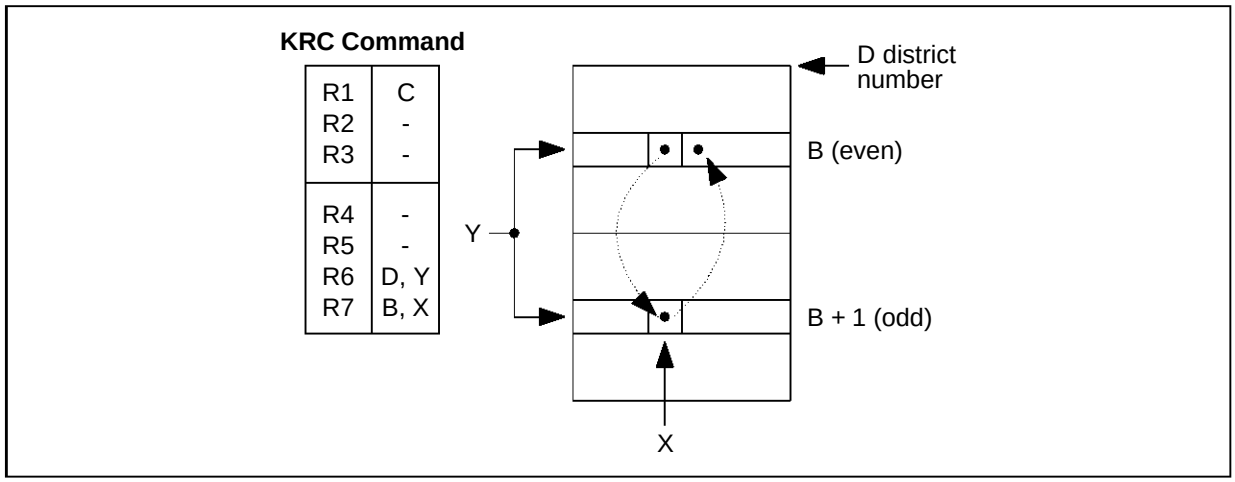


Figure 32 : Transcoding an Horizontal Screen Location into a R7 Pointer

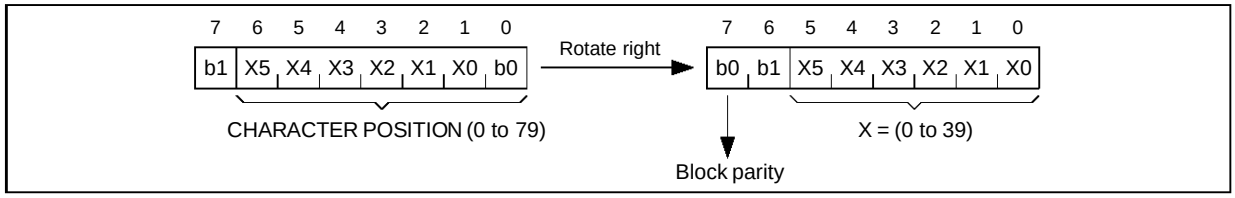
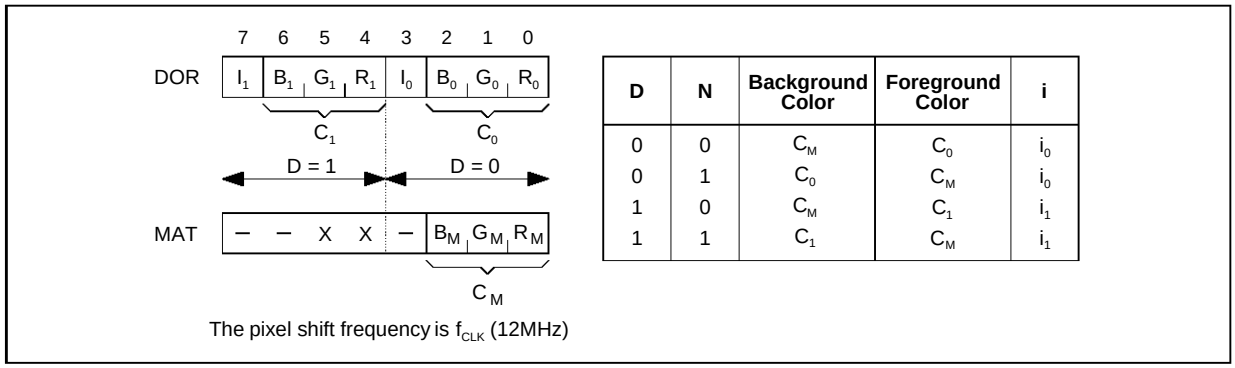


Figure 33

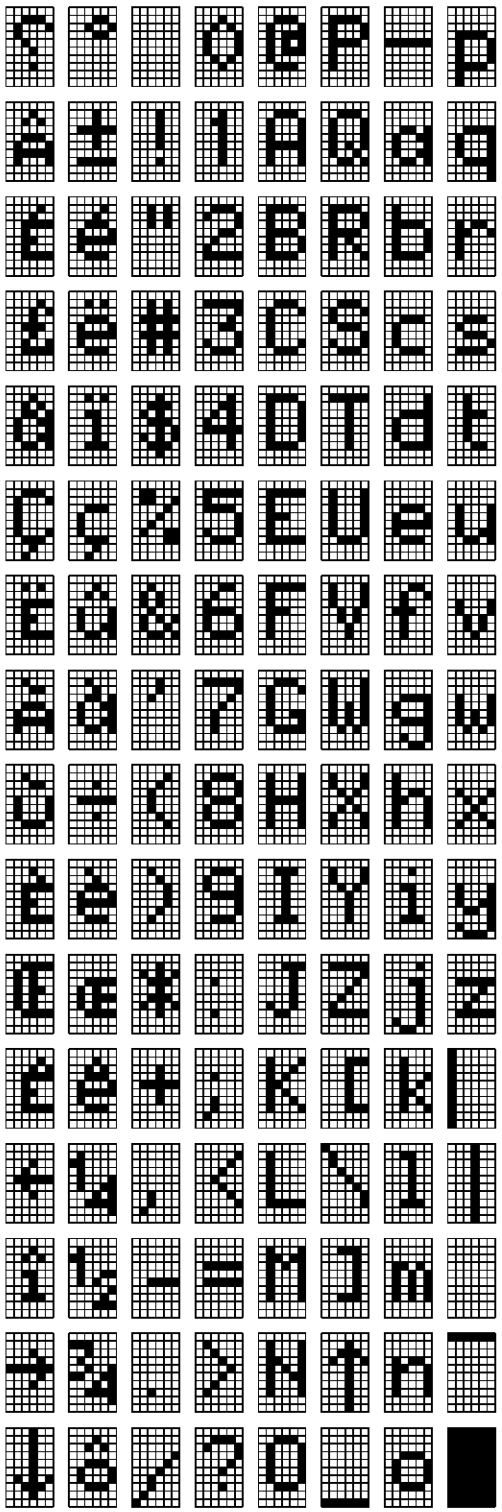


D	N	Background Color	Foreground Color	i
0	0	C_M	C_0	i_0
0	1	C_0	C_M	i_0
1	0	C_M	C_1	i_1
1	1	C_1	C_M	i_1

Figure 34 : G_0 Alphanumeric Character Set in 80 Character/Row Mode

C7	0	0	0	0	0	0	0	0
C6	0	0	0	0	1	1	1	1
C5	0	0	1	1	0	0	1	1
C4	0	1	0	1	0	1	0	1

C3	C2	C1	C0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1



9345-37.EPS

MICROPROCESSOR ACCESS COMMANDS

A microprocessor bus cycle may transfer one byte from/to the microprocessor to/from a directly addressable register. These registers provide an indirect access :

- To/from 5 on-chip indirect registers : ROR, DOR, MAT, PAT and TGS.
- To/from the private memory.

Due to address/data multiplexing, a bus cycle is a 2 phase process (see Timing diagram 1 or Timing diagram 2).

Address Phase

The falling edge of AS latches to AD(0:7) bus state and $\overline{CS}$ signal into the temporary A address register (Figure 36).

- A(0:2) = i :
  This register index designates one out of 8 direct access registers Ri.
- A3 = XQR :
  This is the execution request bit.
- A(4:7) = ASN :
  This is the Auto-Selection Nibble
- A8 = $\overline{LCS}$:
  This is the latched value of $\overline{CS}$ input pin.

EF9345 is selected when the following condition is met : ASN = 2(Hexa) and $\overline{LCS}$ = 0.

Therefore, EF9345 is mapped in the hexadecimal microprocessor addressing space form XX20 to XX2F, where XX is up to the user. Xhen EF9345 is not selected, its AD bus pins float and no register can be modified.

Figure 35

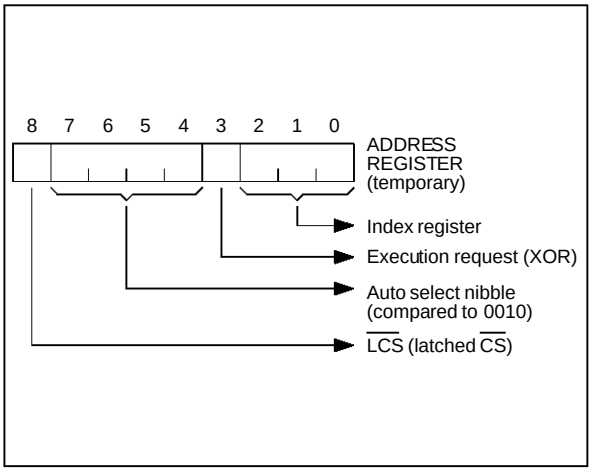
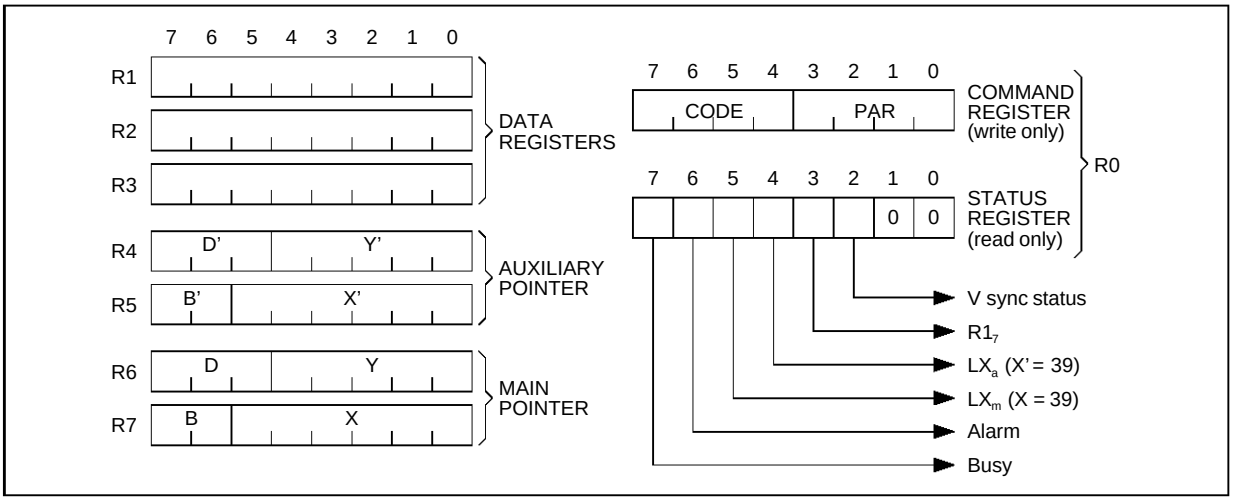


Figure 36 : Direct Access Registers



Data Phase - Registers

When EF9345 is selected and while AS input is low, the Ri register is accessed.

R0 designates a write-only COMMAND register or a read-only STATUS register.

R1 to R7 hold the arguments of a command. They are read/write registers.

R1, R2, R3 are used to transfer the data.

R4, R5 hold the Auxiliary Pointer (AP).

R6, R7 hold the Main Pointer (MP).

(see memory organization ; pinter section for pointer structure).

Command Register

This register holds a 4-bit command type and 4 bits of orthogonal parameters (see command table).

Type

There are 4 groups of command :

The IND command which gives access to on-chip resources,

The fixed format character code transfer commands,

The variable character code handling commands,

The general purpose commands.

Parameters

R/W : Direction
1 : to DATA registers (R1, R2, R3)
0 : from DATA registers.

r : Internal resource index (see figure 27).

I : Auto-incrementation
1 : with post auto-incrementation
0 : without auto-incrementation

p : Pointer select
1 : auxiliary pointer
0 : main pointer

s, $\overline{s}$: Source, destination select
01 : source : MP ; destination : AP
10 : source : AP ; destination : MP

$\overline{a}$, a : Stop condition
01 : stop at end of buffer
10 : no stop.

Status Register

This is a read-only, direct access register.

S7 : BUSY — BUSY is set at the beginning of any command execution. It is reset at completion.

S6 : AI — LXm or LXa is set when respectively the main pointer or the

S5 LX_m — auxiliary pointer holds X = 39 before a possible incrementation.

S4 : LX_a — The alarm bit S6 is set when LXm or LXa is set and an incrementation is performed after access.

S3 : Gives the MSB value of R1.

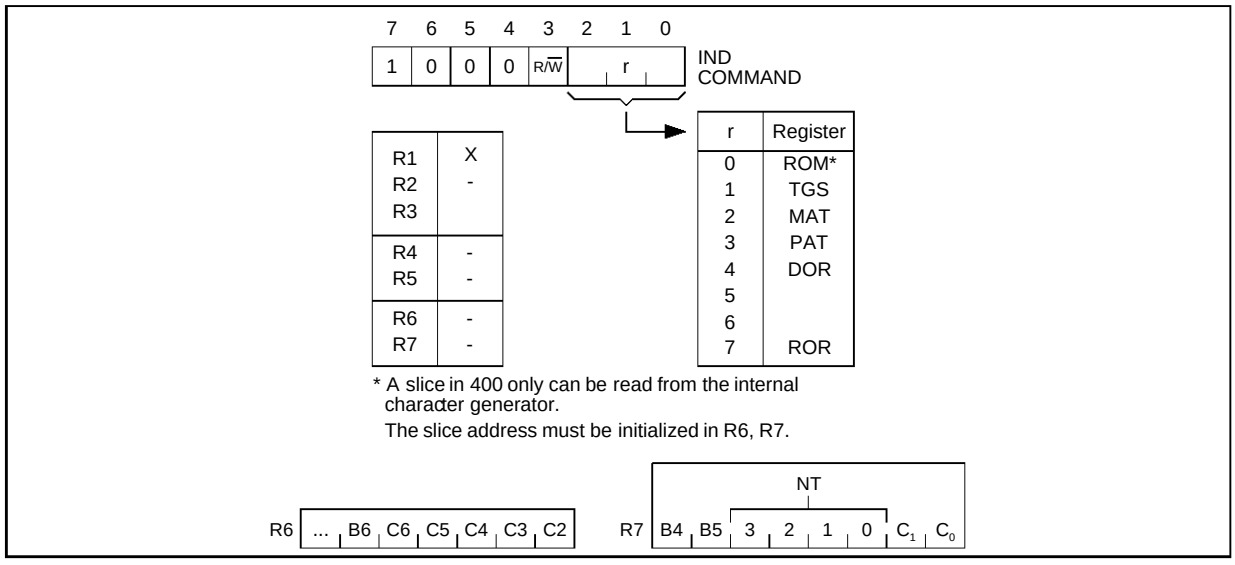
S2 : Gives the vertical synchronization signal state.
This is maskable by the VRM command.

S1 = S0 = 0 Not used.

S3 to S6 are reset at the beginning of any command.

The COMMAND TABLE shows every command able to set, each of these status bits, after completion.

Figure 37 : Indirect On-Chip Resource Access



Notes on Command Execution

1. The execution of any command starts at the trailing edge of DS when (and only when) :
- EF9345 has been selected,
- XQR has been set,
  at the previous AS falling edge.

This scheme allows loading a command and its argument in any order. For instance, a command, once loaded, may be re-executed with new or partly new arguments.

2. At power on, the busy state is undeterminated. It is recommanded to load first a dummy command with XQR = 1 before any effective command.
3. While Busy is set, the current command is under execution. Register access is then restricted.

Register access with XQR = 0
- Read STATUS is effective.
- Write COMMAND or any other register access are ineffective.

That is to say, the microprocessor reads undetermined values and may not modify a register.

Register access with XQR = 1
- Read STATUS or write COMMAND are effective,
- Access to other registers is ineffective.

However, the previous command is aborted and the new command execution launched (with an initial state undetermined for registers and memory locations handled by the aborted command).

4. Execution suspension

The execution of any command (except VRM, VSM) is suspended during the last and first TV line of an active row. This is because the memory bus cannot be allocated for microprocessor access during this 104 µs period.

This holds too for internal resource access because on-chip data transfer uses internal data memory bus.

IND Command (See Figure 37)

This command transfers one byte between R1 and an internal resource. The r parameter designates one on-chip indirect register.

Fixed Format Character Code Access : KRF, KRG, KRL, KRC

Each of these commands is dedicated to transfer one complete character code between DATA registers and memory. MP is exclusively used.

KRF transfers 24 bits.

KRG transfers 16 bits

KRL transfers 12 bits.

KRC transfers 8 bits.

Code packing, pointer and data structures are explained in the corresponding character code section.

When auto-incrementation is enabled, MP is automatically updated after access so as to point to the next location. This location corresponds to the next right position on screen. When last position (X = 39) is accessed, LXm is set. When last position is accessed with auto-incrementation, alarm is also set. MP is then pointing back at the beginning of the row : there is no automatic Y incrementation.

Variable Code Handling Commands : KRV EXP, CMP, KRE

An overview on these commands is given in "handling the variable codes" (40 char./row section).

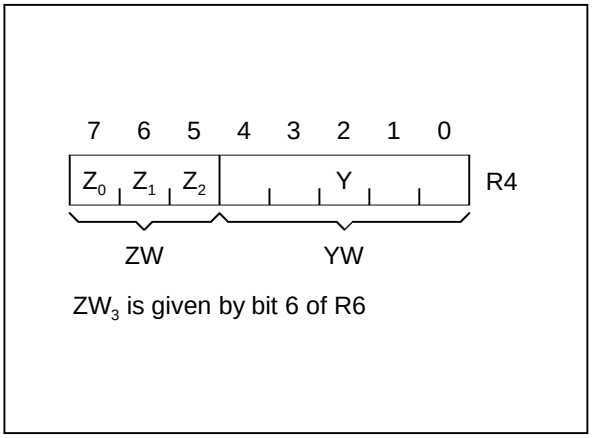
KRV uses R5 to point the attribute file. LX_a is set when this file is full (the last attribute pair has been accessed).

EXP and CMP use MP and R5 in the same way as KRV. Furthermore, R4 points to a working double buffer. Thse two commands process a whole row buffer and stop either at the end of the row buffer or when the file overflows. In the last case, the alarm bit is set.

KRE uses MP to point to a buffer and R4 to point to a working double buffer. R5 is unused. In other respects, KRE is identical to KRL.

For these commands, R4(5:7) hold the LSB's block dress of the working buffer W.

Figure 38



General Purpose Access to a Byte OCT

This command uses either MP or AP pointer.

When MP is in use, an overflow yields to a Y incrementation.

Move Buffer Commands : MVB, MVD, MVT

These are memory to memory commands which use R1 as working register.

MVB transfers a byte from source to destination, post-increments the 2 pointers and iterates until the stop condition is met. MVD and MVT are similar but work respectively with 2 byte word and 3 byte word. That is to say, MVB works on buffers, MVD on double buffers and MVT on triple buffers. If the parameter a = 1, the process stops when either source or destination buffer end is reached. If the parameter a = 0, the process never stops until aborted. In this case, main pointer overflow yields to a Y incrementation in MP. So, a whole block or page may be initialized.

Miscellaneous Commands : INY, VRM and VSM

INY command increments Y in MP.

VRM and VSM respectively reset and set a vertical synchronization status mask. When the mask is set, status bit S2 remains at 0. When the mask is reset, status S2 follows the vertical sync. state : it is reset for 2 TV lines per frame and stays at 1 during the remaining period. It becomes readable by the microprocessor form the status register. After power on, the mask state is undetermined.

Table 4 : Command

Type	Memo	Code				Parameter				Status				Arguments							Execution Time (1)	
		7	6	5	4	3	2	1	0	AI	LX_m	LX_a	R17	R1	R2	R3	R4	R5	R6	R7	Write	Read
Indirect	IND	1	0	0	0	R/$\overline{W}$		r		0	0	0	0	D	-	-	-	-	MP		2	3.5
40 Characters - 24 bits	KRF	0	0	0	0	R/$\overline{W}$	0	0	I	X	X	0	0	C	B	A	-	-	MP		4	7.5
40 Characters - 16 bits	KRG	0	0	0	0	R/$\overline{W}$	0	1	I	X	X	0	0	A*	B*	W	-	-	MP		5.5	7.5
80 Characters - 8 bits	KRC	0	1	0	0	R/$\overline{W}$	0	0	I	X	X	0	0	C	-	-	-	-	MP		9	9.5
80 Characters - 12 bits	KRL	0	1	0	1	R/$\overline{W}$	0	0	I	X	X	0	0	C	-	A	-	-	MP		12.5	11.5
40 Characters Variable	KRV	0	0	1	0	R/$\overline{W}$	0	0	I	X	X	X	X	C	B	A	-	XF	MP		(2) 3 + 3 + j	3.5 + 6 * j
Expansion	EXP	0	1	1	0	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP		(3) < 247	-
Compression	CMP	0	1	1	1	0	0	0	0	X	0	X	0	C	B	A	PW	XF	MP		(3) < 402	-
Expanded Characters	KRE	0	0	0	1	R/$\overline{W}$	0	0	I	X	X	0	0	C	B	A	PW	-	MP		4	7.5
Byte	OCT	0	0	1	1	R/$\overline{W}$	p	0	I	X	X	X	0	D	-	-	AP		MP		4	4.5
Move Buffer	MVB	1	1	0	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	-	-	AP		MP		(2) 2 + 4. n	-
Move Double Buffer	MVD	1	1	1	0	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	-	-	AP		MP		(2) 2 + 8. n	-
Move Triple Buffer	MVT	1	1	1	1	s	$\overline{s}$	$\overline{a}$	a	0	0	0	0	W	-	-	AP		MP		(2) 2 + 12. n	-
Clear Page (4) - 24 Bits	CLF	0	0	0	0	0	1	0	1	X	X	0	0	C	B	A	-	-	MP		< 4700 (1 K code)	-
Clear Page (4) - 16 bits	CLG	0	0	0	0	0	1	1	1	X	X	0	0	A*	B*	W	-	-	MP		< 5800 (1 K code)	-
Vertical Sync Mask Set	VSM	1	0	0	1	1	0	0	1	0	0	0	0	-	-	-	-	-	-	-	1	-
Vertical Sync Mask Reset	VRM	1	0	0	1	0	1	0	1	-	-	-	-	-	-	-	-	-	-	-	1	-
Increment Y	INY	1	0	1	1	0	0	0	0	0	0	0	0	-	-	-	-	-	Y	-	2	-
No Operation	NOP	1	0	0	1	0	0	0	1	-	-	-	-	-	-	-	-	-	-	-	1	-

9345-09.TBL

P : Pointer select
1 : auxiliary pointer
0 : main pointer

s, $\overline{s}$: Source, destination
01 : source = MP ; destination = AP
10 : source = AP ; destination = MP

$\overline{a}$, a : Stop condition
01 : stop at end of buffer
10 : no stop

r : Indirect register number

\- : Not affected

W : Used as working register

PW (Z, YW) : Working buffer

X : Set or Reset

XF : X File

I : Pointer incrementation

D : Data

MP : Main pointer

AP : Auxiliary pointer

(1) Unit : 12 clock periods (≈ 1µs) without possible suspension.

(2) n : total number of word ≤ 40 ; j = 1 for long code, j = 0 for short codes.

(3) : Worst case (20 long codes + 20 short codes).

(4) : These commands repeats KRF or KRG with Y incrementation when X overflows. When the last position is reached in a row. Y is incremented and the process starts again on the next row.

Figure 39 : Interface with EF6801

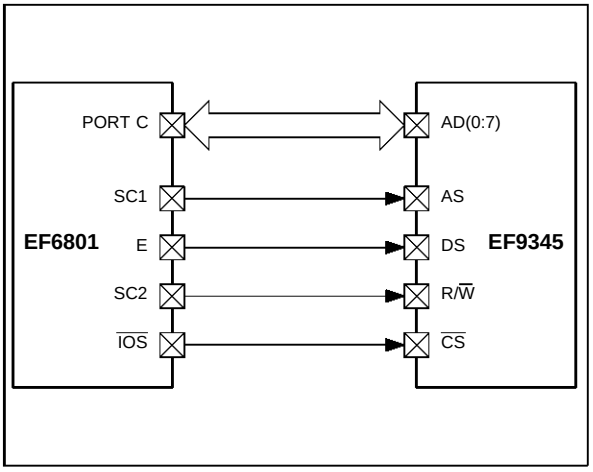


Figure 40 : Minimum Application with 2K x 8 Memory

One page memory terminal in 16-bit fixed format or 24-bit compressed format.

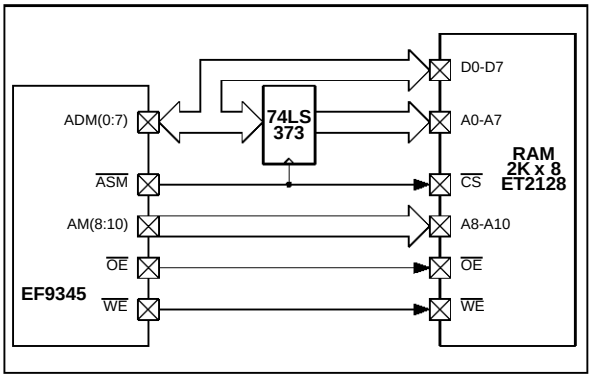


Figure 41 : Typical Application with 8K x 8 Dynamic or Pseudoi-static RAM

Multipage terminal with possibility of multiple user definable character sets.

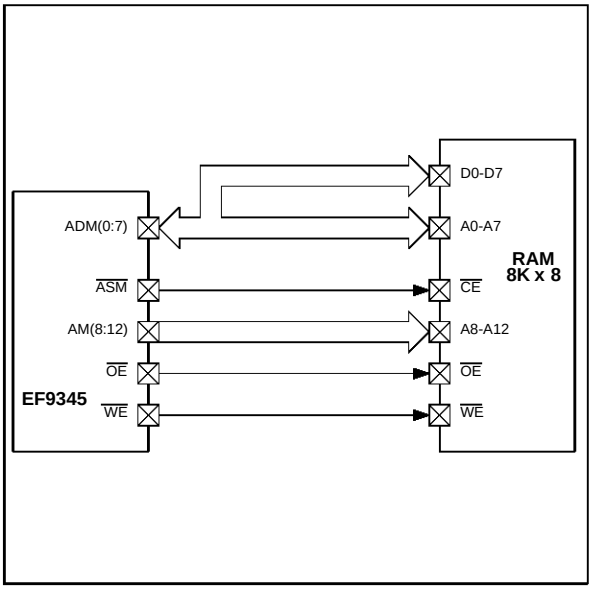
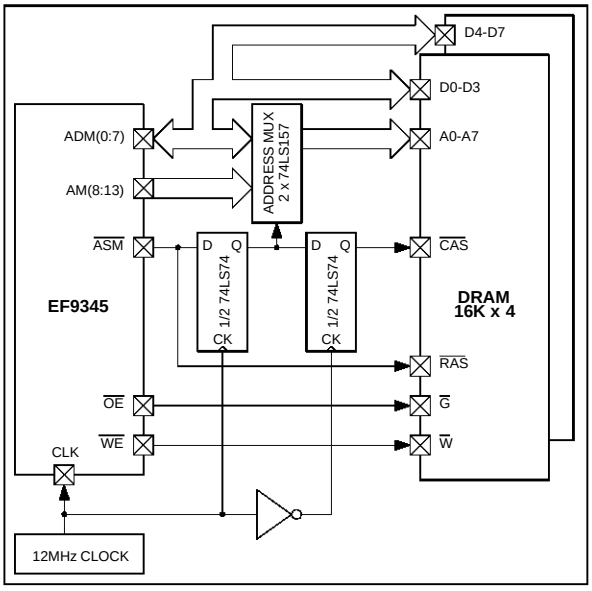


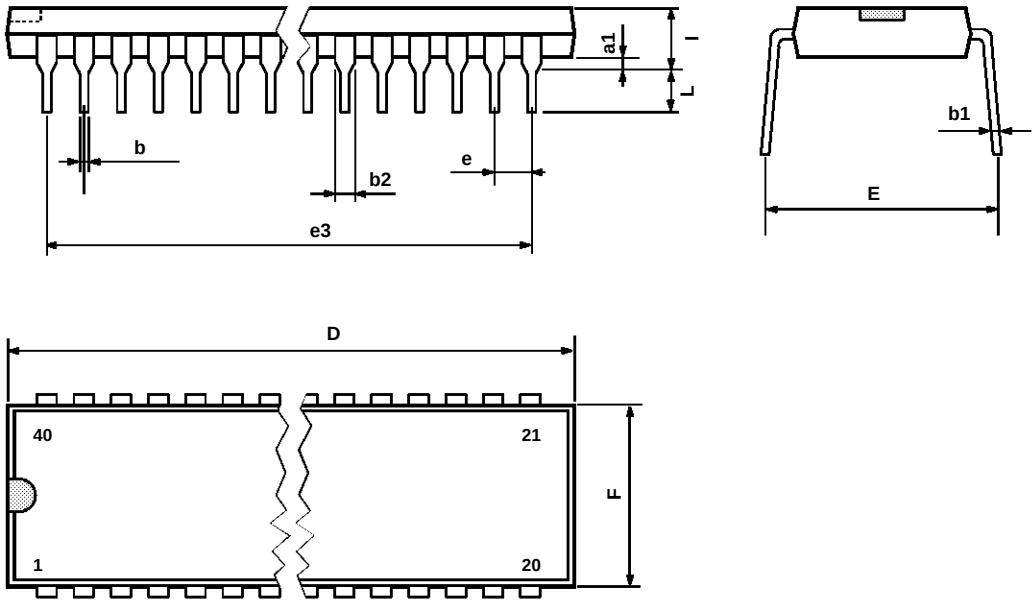
Figure 42 : Maximum Application with 16K x 8 Memory

Multipage terminal with user definable character sets and buffer areas.



PACKAGE MECHANICAL DATA

40 PINS - PLASTIC DIP



PM-DIP40.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

DIP40.TBL