U.H.F. POWER TRANSISTOR

N-P-N silicon planar epitaxial transistor designed for use in mobile radio transmitters in the 900 MHz band.

Features:

- emitter-ballasting resistors for an optimum temperature profile
- gold metallization ensures excellent reliability.

The transistor is encapsulated in a subminiature plastic transfer-moulded cross package (SOT-103).

QUICK REFERENCE DATA

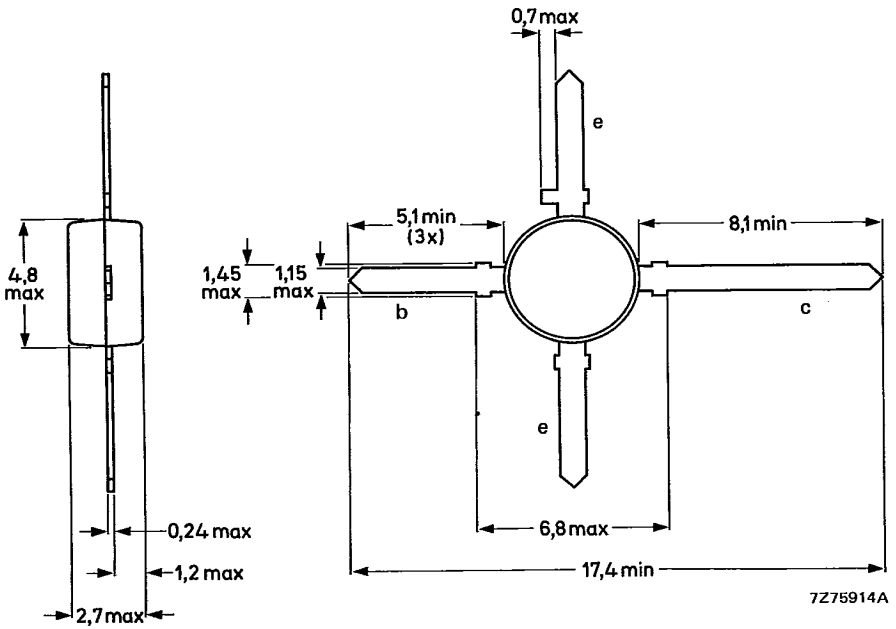
R.F. performance at T_{amb} = 25 °C in a common-emitter class-B circuit

mode of operation	V_{CE} V	f MHz	P_L W	G_P dB	η_C %
narrow band; c.w.	12,5	900	0,5	> 8,0	> 50

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT-103.



RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Collector-base voltage (open emitter)	V_{CBO}	max.	36 V
Collector-emitter voltage (open base)	V_{CEO}	max.	16 V
Emitter-base voltage (open collector)	V_{EBO}	max.	3 V
Collector current			
d.c. or average	I_C	max.	150 mA
(peak value); f > 1 MHz	I_{CM}	max.	500 mA
Total power dissipation at $T_{coll.\ tap}$ = 75 °C	P_{tot}	max.	1,65 W
Total power dissipation* at T_{amb} = 25 °C	P_{tot}	max.	1,0 W
Storage temperature	T_{stg}		−65 to +150 °C
Operating junction temperature	T_j	max.	175 °C

THERMAL RESISTANCE*

From junction to collector tap (d.c.)	$R_{th\ j\text{-}ct(dc)}$	=	60 K/W
From junction to ambient (d.c.)	$R_{th\ j\text{-}a(dc)}$	=	150 K/W

CHARACTERISTICS

T_j = 25 °C unless otherwise specified

Collector-base breakdown voltage open emitter; I_C = 2,5 mA	$V_{(BR)CBO}$	>	36 V
Collector-emitter breakdown voltage open base; I_C = 10 mA	$V_{(BR)CEO}$	>	16 V
Emitter-base breakdown voltage open collector; I_E = 0,5 mA	$V_{(BR)EBO}$	>	3 V
Collector cut-off current V_{BE} = 0; V_{CE} = 16 V	I_{CES}	<	1 mA
D.C. current gain I_C = 100 mA; V_{CE} = 10 V	h_{FE}	>	25
Transition frequency at f = 500 MHz** $-I_E$ = 100 mA; V_{CB} = 12,5 V	f_T	typ.	4,0 GHz
Collector capacitance at f = 1 MHz $I_E = i_e$ = 0; V_{CB} = 12,5 V	C_c	typ.	2,1 pF
Feed-back capacitance at f = 1 MHz I_C = 0; V_{CE} = 12,5 V	C_{re}	typ.	1,3 pF

* Transistor mounted on a p.c. board with a collector area of 50 mm².
** Measured under pulse conditions: t_p = 50 μs; δ < 1%.

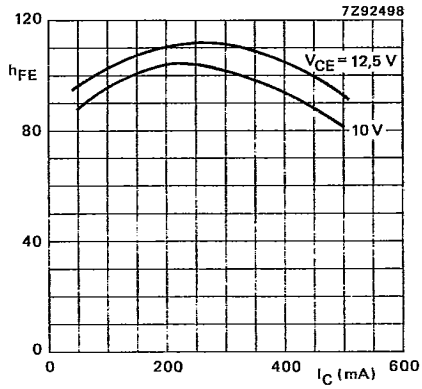


Fig. 2 T_j = 25 °C; typical values.

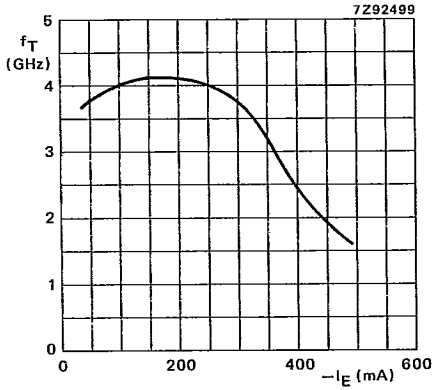


Fig. 3 V_{CB} = 12,5 V; f = 500 MHz; T_j = 25 °C; typical values.

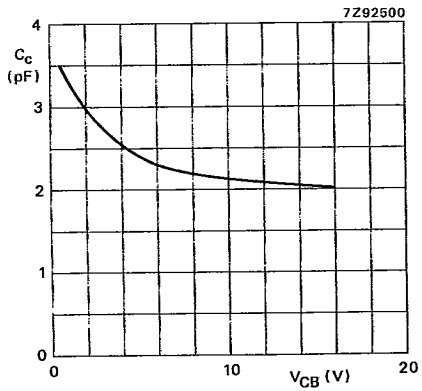


Fig. 4 $I_E = i_e = 0$; f = 1 MHz; typical values.

APPLICATION INFORMATION

R.F. performance in c.w. operation (common-emitter circuit; class-B): f = 900 MHz; T_{amb} = 25 °C

mode of operation	V_{CE} V	P_L W	P_S W	G_P dB	I_C mA	η_C %
narrow band; c.w.	12,5	0,5	< 0,079 typ. 0,056	> 8,0 typ. 9,5	< 80 typ. 62	> 50 typ. 65

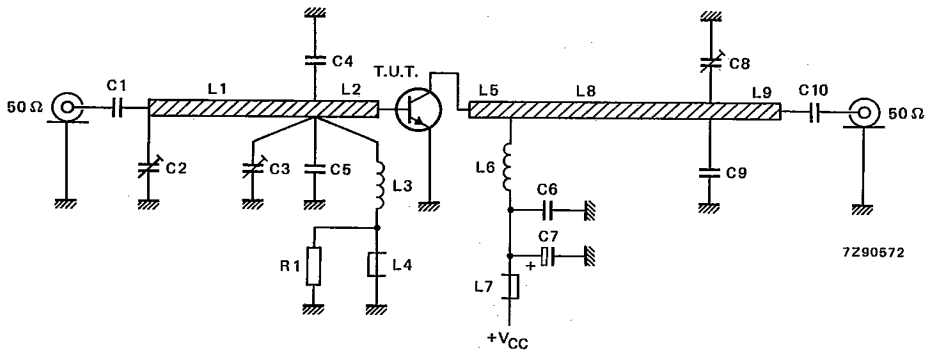


Fig. 5 Class-B test circuit at f = 900 MHz.

List of components:

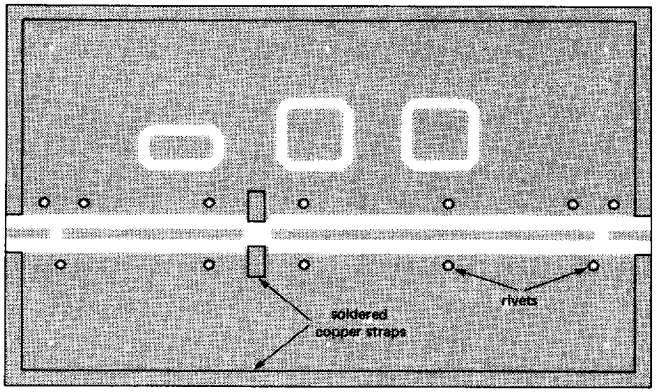
C1 = C6 = C10 = 330 pF multilayer ceramic chip capacitor
C2 = C3 = 1,4 to 5,5 pF film dielectric trimmer (cat. no. 2222 809 09001)
C4 = C5 = 6,8 pF multilayer ceramic chip capacitor*
C7 = 6,8 μF (63 V) electrolytic capacitor
C8 = 1,0 to 3,5 pF film dielectric trimmer (cat. no. 2222 809 05001)
C9 = 1,2 pF multilayer ceramic chip capacitor*

L1 = 50 Ω stripline (24,0 mm x 2,4 mm)
L2 = 50 Ω stripline (8,0 mm x 2,4 mm)
L3 = 60 nH; 4 turns closely wound enamelled Cu wire (0,4 mm); int. dia. 3 mm; leads 2 x 5 mm
L4 = L7 = Ferroxcube wideband h.f. choke, grade 3B (cat. no. 4312 020 36642)
L5 = 50 Ω stripline (14,0 mm x 2,4 mm)
L6 = 245 nH; 9 turns closely wound enamelled Cu wire (1,0 mm); int. dia. 5 mm; leads 2 x 3 mm
L8 = 50 Ω stripline (32,5 mm x 2,4 mm)
L9 = 50 Ω stripline (10,0 mm x 2,4 mm)

R1 = 10 Ω ± 10%; 0,25 W metal film resistor

L1, L2, L5, L8 and L9 are striplines on a double Cu-clad printed circuit board with P.T.F.E. fibre-glass dielectric (ϵ_r = 2,2); thickness 1/32 inch.

* American Technical Ceramics capacitor type 100A or capacitor of same quality.



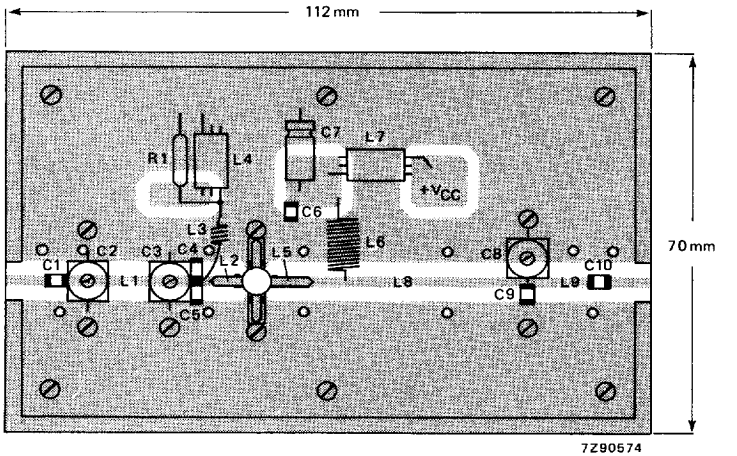


Fig. 6 Printed circuit board and component lay-out for 900 MHz class-B test circuit.

Note

The circuit and the components are on one side of P.T.F.E. fibre-glass board; the other side is unetched copper serving as ground plane. Earth connections are made by fixing-screws and copper straps around the board and under the emitters to provide a direct contact between the copper on the component side and the ground plane.

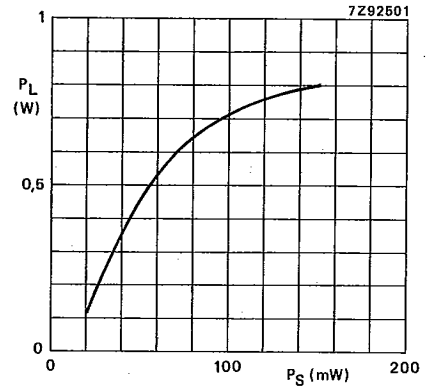


Fig. 7 Load power vs. source power.

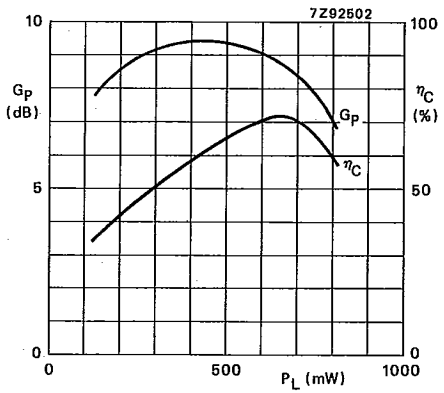


Fig. 8 Power gain and efficiency vs. load power.

Conditions for Figs 7 and 8:

V_{CE} = 12;5 V; f = 900 MHz; T_{amb} = 25 °C; class-B operation; test circuit tuned at P_L = 0,5 W; typical values.

RUGGEDNESS

The transistor is capable of withstanding a full load mismatch (VSWR = 50; all phases) at rated load power up to a supply voltage of 15,5 V and T_{amb} = 25 °C.

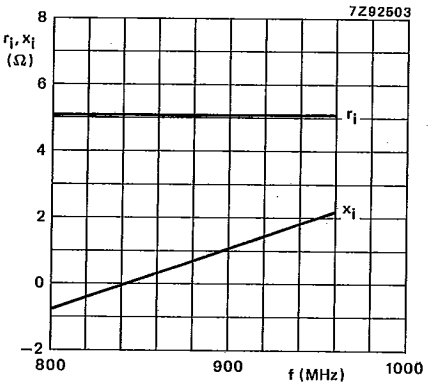


Fig. 9 Input impedance (series components).

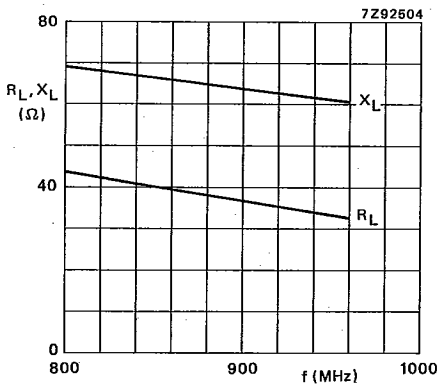


Fig. 10 Load impedance (series components).

Conditions for Figs 9 and 10:

V_{CE} = 12,5 V; P_L = 0,5 W; f = 800-960 MHz; T_{amb} = 25 °C; class-B operation; typical values.

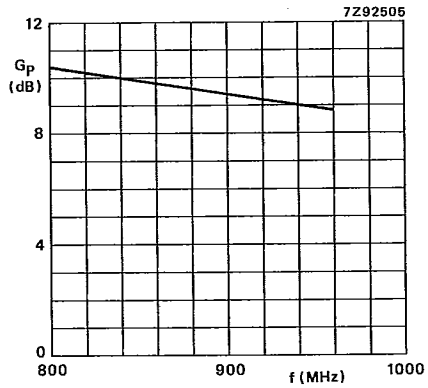


Fig. 11 Power gain vs. frequency.

V_{CE} = 12,5 V; P_L = 0,5 W; f = 800-960 MHz; T_{amb} = 25 °C; class-B operation; typical values.