High Performance
256K×16
CMOS DRAM

AS4C256K16F0

High Speed 256K×16 CMOS DRAM (Fast Page Mode)

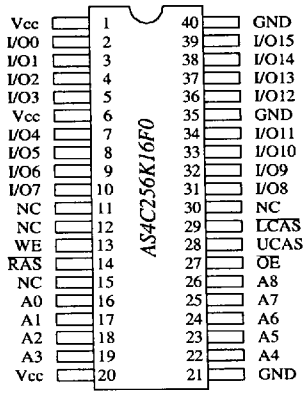
PRELIMINARY

FEATURES

- Organization: 262,144 words by 16 bits
- High speed
  - 50/60 ns $\overline{RAS}$ access time
  - 25/30 ns column address access time
  - 14/15 ns $\overline{CAS}$ access time
- Low power consumption
  - Active: 715 mW max (4C256K16F0-50)
  - Standby: 5.5 mW max, CMOS I/O
- Fast page mode
- 512 refresh cycles, 8 ms refresh interval
  - $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh
- Read-modify-write
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400 mil, 40-pin SOJ
- Single 5V power supply / built-in V_{bb} generator

PIN ARRANGEMENT

SOJ



PIN DESIGNATION

Pin(s)	Description
A0 to A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
I/O0 to I/O15	Input/Output
$\overline{OE}$	Output Enable
$\overline{UCAS}$	Column Address Strobe, Upper Byte
$\overline{LCAS}$	Column Address Strobe, Lower Byte
$\overline{WE}$	Read/Write Control
V_{CC}	Power (+5V ± 10%)
GND	Ground

SELECTION GUIDE

	Symbol	4C256K16F0-50	4C256K16F0-60	Unit
Maximum $\overline{RAS}$ Access Time	t_{RAC}	50	60	ns
Maximum Column Address Access Time	t_{AA}	25	30	ns
Maximum $\overline{CAS}$ Access Time	t_{CAC}	14	15	ns
Maximum Output Enable ($\overline{OE}$) Access Time	t_{OEA}	14	15	ns
Minimum Read or Write Cycle Time	t_{RC}	85	110	ns
Minimum Fast Page Mode Cycle Time	t_{PC}	30	35	ns
Maximum Operating Current	I_{CC1}	130	110	mA
Maximum CMOS Standby Current	I_{CC5}	1.0	1.0	mA

FUNCTIONAL DESCRIPTION

The AS4C256K16F0 is a high performance 4 megabit CMOS Dynamic Random Access Memory (DRAM) organized as 262,144 words by 16 bits. The AS4C256K16F0 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

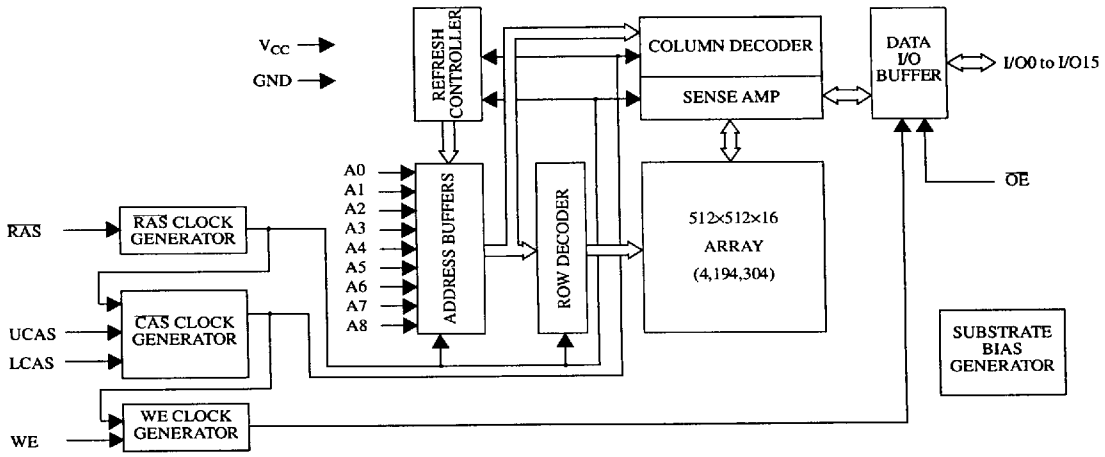
The AS4C256K16F0 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the 512 × 16 bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Output is tri-stated by a column address strobe ($\overline{CAS}$) which acts as an output enable independent of $\overline{RAS}$. Very fast $\overline{CAS}$ to output access time eases system design.

Refresh on the 512 address combinations of A0 to A8 during an 8 ms period is accomplished by performing any of the following:

- $\overline{RAS}$-only refresh cycles
- Hidden refresh cycles
- $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles
- Normal read or write cycles

The AS4C256K16F0 is available in a standard 40-pin plastic SOJ packages compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ± 10% tolerance and direct interface with TTL logic families.

LOGIC BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS (T_a = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0.0	0.0	0.0	V
Input Voltage	V_{IH}	2.4	–	V_{CC}	V
	V_{IL}	–0.5†	–	0.8	V

†V_{IL} min -3.0V for pulse widths less than 5 ns.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Input Voltage	V_{in}	-1.0	+7.0	V
Input Voltage (I/Os)	$V_{I/O}$	-1.0	V_{CC} + 0.5	V
Power Supply Voltage	V_{CC}	-1.0	+7.0	V
Operating Temperature	T_{OPR}	0	+70	°C
Storage Temperature (Plastic)	T_{STG}	-55	+150	°C
Soldering Temperature × Time	T_{SOLDER}	–	260 × 10	°C × sec
Power Dissipation	P_D	–	1	W
Short Circuit Output Current	I_{out}	–	50	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5 ± 10%, GND = 0V, T_a = 0°C to +70°C)

Parameter	Symbol	Test Conditions	-50		-60		Unit	Notes
			Min	Max	Min	Max		
Input Leakage Current	I_{IL}	0V ≤ V_{in} ≤ +5.5V Pins Not Under Test = 0V	-10.0	+10.0	-10.0	+10.0	µA	
Output Leakage Current	I_{OL}	D_{OUT} Disabled, 0V ≤ V_{out} ≤ +5.5V	-10.0	+10.0	-10.0	+10.0	µA	
Operating Power Supply Current	I_{CC1}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Address Cycling; t_{RC}=min	–	130	–	110	mA	1,2
TTL Standby Power Supply Current	I_{CC2}	$\overline{RAS}$ = $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}	–	2.0	–	2.0	mA	
Average Power Supply Current, $\overline{RAS}$ Refresh Mode	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{UCAS}$ = $\overline{LCAS}$ = V_{IH}, t_{RC} = min	–	130	–	110	mA	1
Fast Page Mode Average Power Supply Current	I_{CC4}	$\overline{RAS}$=V_{IL}, $\overline{UCAS}$=$\overline{LCAS}$, Address Cycling: t_{PC} = min	–	70	–	65	mA	1,2
CMOS Standby Power Supply Current	I_{CC5}	$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$= V_{CC} - 0.2V	–	1.0	–	1.0	mA	
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Power Supply Current	I_{CC6}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, Cycling; t_{RC} = min	–	130	–	110	mA	1
Output Voltage	V_{OH}	I_{OUT} = -5.0 mA	2.4	–	2.4	–	V	
	V_{OL}	I_{OUT} = 4.2 mA	–	0.4	–	0.4	V	

Shaded areas contain advance information.

AC PARAMETERS COMMON TO ALL WAVEFORMS

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Std Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	–	5	–	ns	
t_{RC}	Random Read or Write Cycle Time	85	–	110	–	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	30	–	40	–	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	60	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	8	10K	12	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	15	35	20	45	ns	6
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	25	15	30	ns	7
t_{RSH}	$\overline{CAS}$ to $\overline{RAS}$ Hold Time	10	–	15	–	ns	
t_{CSH}	$\overline{RAS}$ to $\overline{CAS}$ Hold Time	50	–	60	–	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	–	5	–	ns	
t_{ASR}	Row Address Setup Time	0	–	0	–	ns	
t_{RAH}	Row Address Hold Time	9	–	10	–	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	4,5
t_{REF}	Refresh Period	–	8	–	8	ms	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	–	30	–	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	9	–	10	–	ns	

Shaded areas contain advance information.

READ CYCLE

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Std Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	–	50	–	60	ns	6
t_{CAC}	Access Time from $\overline{CAS}$	–	14	–	15	ns	6,13
t_{AA}	Access Time from Address	–	25	–	30	ns	7,13
t_{AR}	Column Add Hold from $\overline{RAS}$	30	–	40	–	ns	
t_{RCS}	Read Command Setup Time	0	–	0	–	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	–	0	–	ns	9
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	–	0	–	ns	9
t_{OFF}	Output Buffer Turn-Off Time	0	13	0	15	ns	8,10

Shaded areas contain advance information.

WRITE CYCLE

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Std Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{ASC}	Column Address Setup Time	0	–	0	–	ns	
t_{CAH}	Column Address Hold Time	9		10		ns	
t_{WCS}	Write Command Setup Time	0	–	0	–	ns	11
t_{WCH}	Write Command Hold Time	9	–	10	–	ns	11
t_{WP}	Write Command Pulse Width	9	–	10	–	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12	–	15	–	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	11	–	15	–	ns	
t_{DS}	Data-In Setup Time	0	–	0	–	ns	12
t_{DH}	Data-In Hold Time	9	–	10	–	ns	12

Shaded areas contain advance information.

READ-MODIFY-WRITE CYCLE

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Std Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Write Cycle Time	130	–	150	–	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	–	80	–	ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	–	40	–	ns	11
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	–	55	–	ns	11

Shaded areas contain advance information.

FAST PAGE MODE CYCLE

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Std Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{PC}	Read *or* Write Cycle Time (Fast Page)	30	–	35	–	ns	14
t_{CPA}	Access Time from CAS Precharge	–	30	–	35	ns	13
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page)	9	–	10	–	ns	
t_{PRWC}	Fast Page Mode RMW Cycle	70	–	80	–	ns	
t_{CRW}	Page Mode $\overline{CAS}$ Pulse Width (RMW)	50	–	50	–	ns	
t_{RASP}	RAS Pulse Width	50	100K	60	100K	ns	

Shaded areas contain advance information.

REFRESH CYCLE

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Std Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$)	5	–	5	–	ns	3
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$)	10	–	10	–	ns	3
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	–	5	–	ns	
t_{CPT}	$\overline{CAS}$ Precharge Time ($\overline{CAS}$-before-$\overline{RAS}$ Counter Test)	10		10		ns	

Shaded areas contain advance information.

OUTPUT ENABLE

(V_{CC} = 5V±10%, GND = 0V, T_a = 0°C to +70°C)

Std Symbol	Parameter	-50		-60		Unit	Notes
		Min	Max	Min	Max		
t_{CLZ}	$\overline{CAS}$ to Output in Low Z	3	–	3	–	ns	8
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	9	–	10	–	ns	
t_{OEA}	$\overline{OE}$ Access Time	–	14	–	15	ns	
t_{OED}	$\overline{OE}$ to Data Delay	14	–	15	–	ns	
t_{OEZ}	Output Buffer Turnoff Delay from $\overline{OE}$	–	14	–	15	ns	8
t_{OEH}	$\overline{OE}$ Command Hold Time	10	–	10	–	ns	

Shaded areas contain advance information.

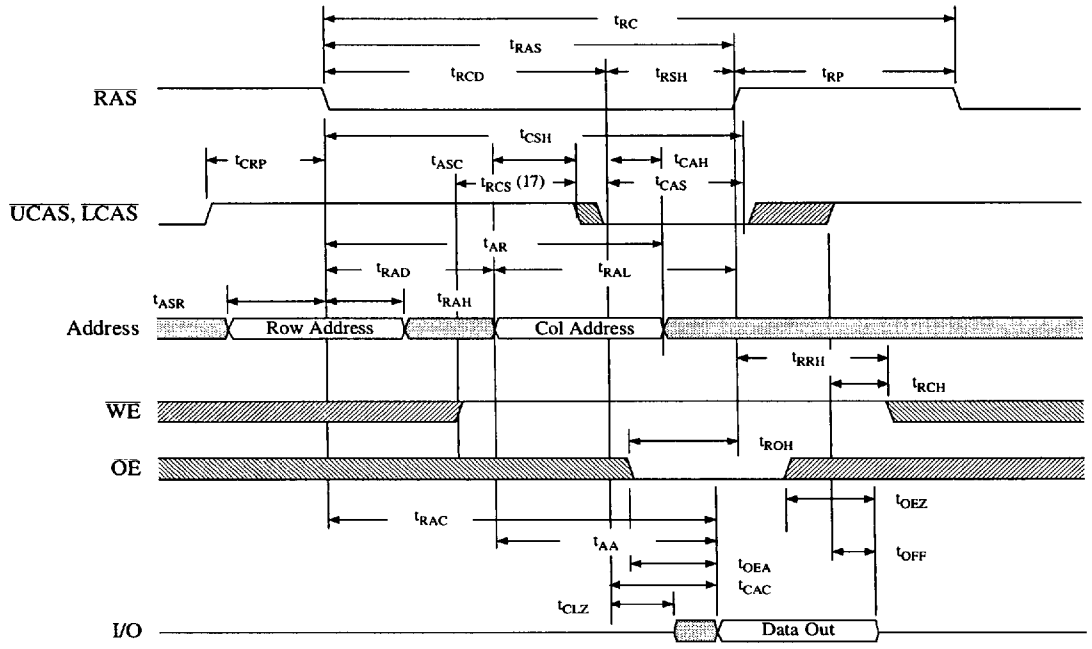
NOTES

1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200 µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8 ms).
4. AC Characteristics assume t_T = 5 ns. All AC parameters are measured with a load equivalent to two TTL loads and 100 pF, V_{IL} (min) ≥ GND and V_{IH} (max) ≤ V_{CC}.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
7. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5 pF and a 380 Ω Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition; it is not referenced to output voltage levels.
11. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only. If t_{WS} ≥ t_{WS} (min) and t_{WH} ≥ t_{WH} (min), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If t_{RWD} ≥ t_{RWD} (min), t_{CWD} ≥ t_{CWD} (min) and t_{AWD} ≥ t_{AWD} (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-write cycles.
13. Access time is determined by the longest of t_{CAA} or t_{CAC} or t_{CPA}.
14. t_{ASC} ≥ t_{CP} to achieve t_{PC} (min) and t_{CPA} (max) values.
15. These parameters are sampled and not 100% tested.

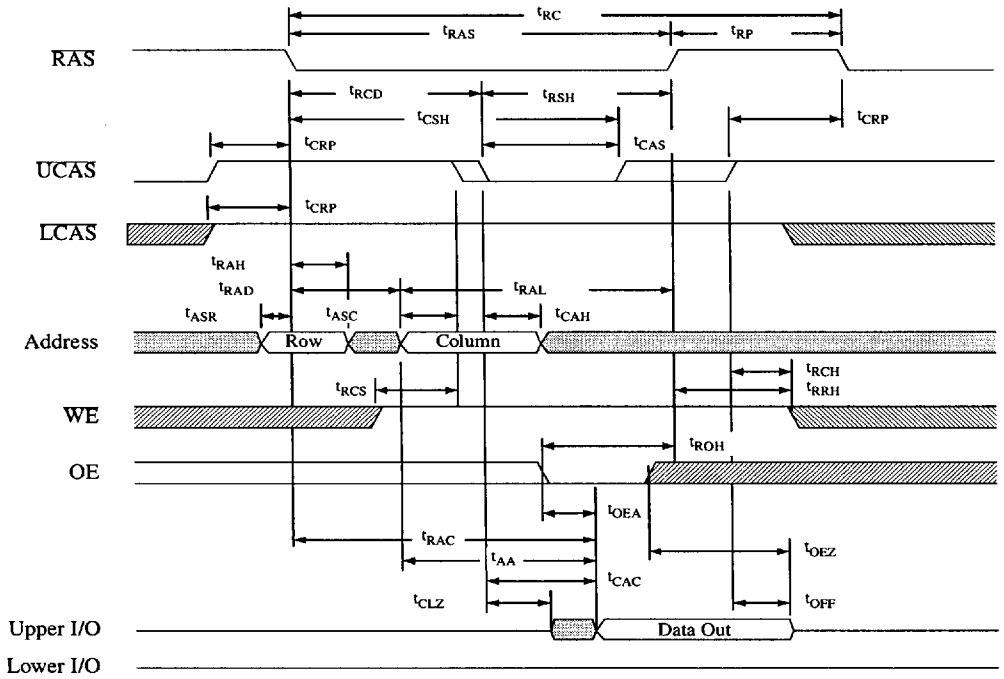
KEY TO SWITCHING WAVEFORMS

Don't Care Input | Rising Input | Falling Input | Undefined Output

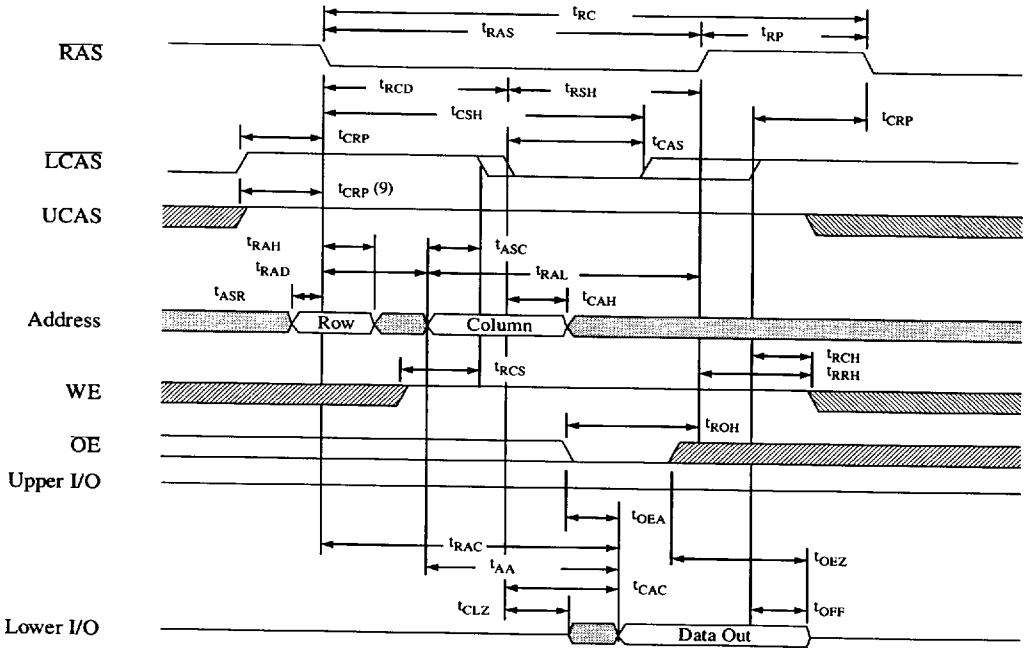
TIMING WAVEFORM OF READ CYCLE



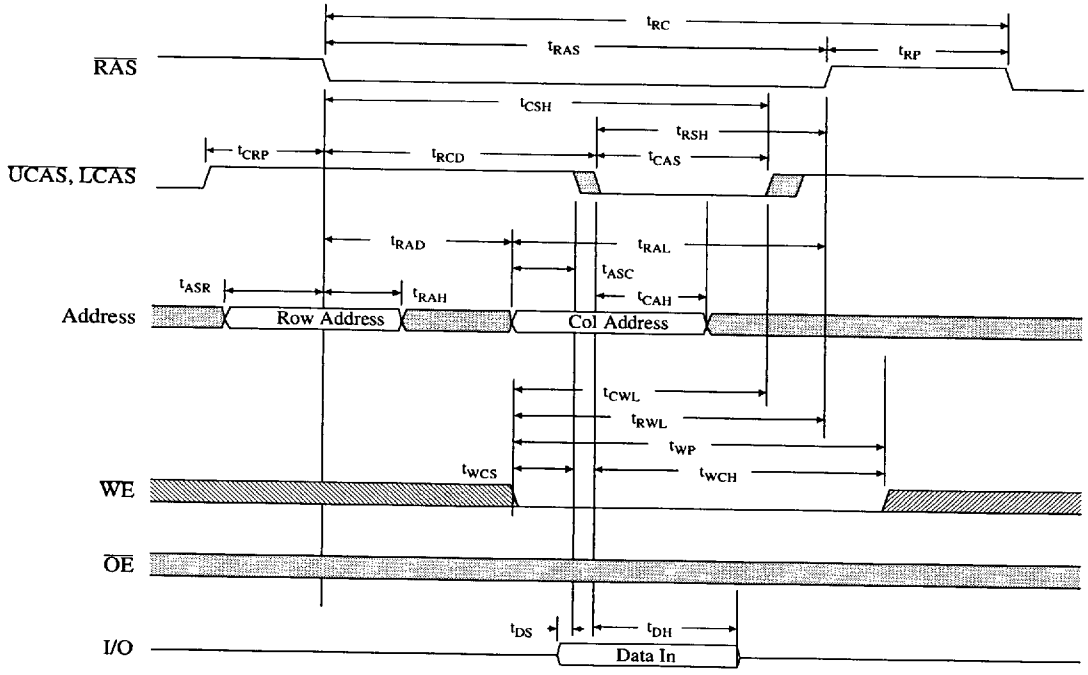
TIMING WAVEFORM OF UPPER BYTE READ CYCLE



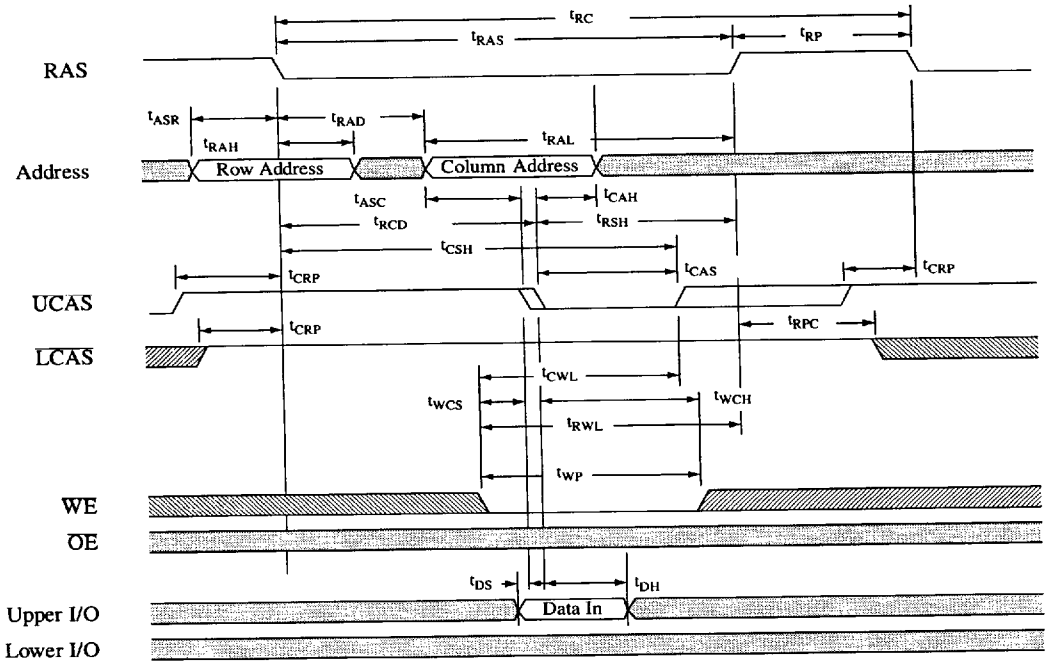
TIMING WAVEFORM OF LOWER BYTE READ CYCLE



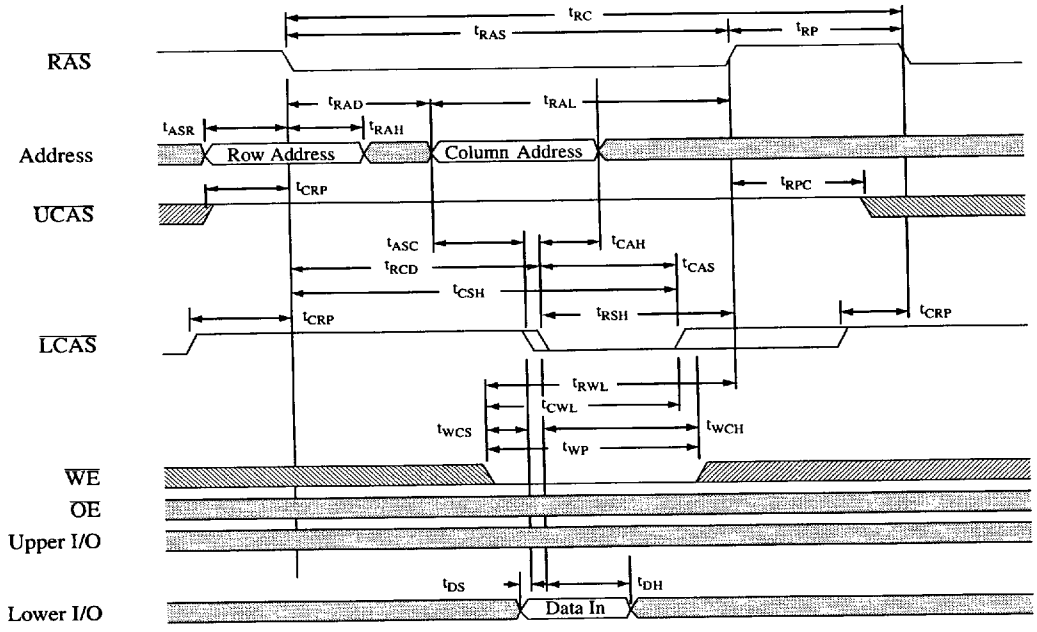
TIMING WAVEFORM OF EARLY WRITE CYCLE



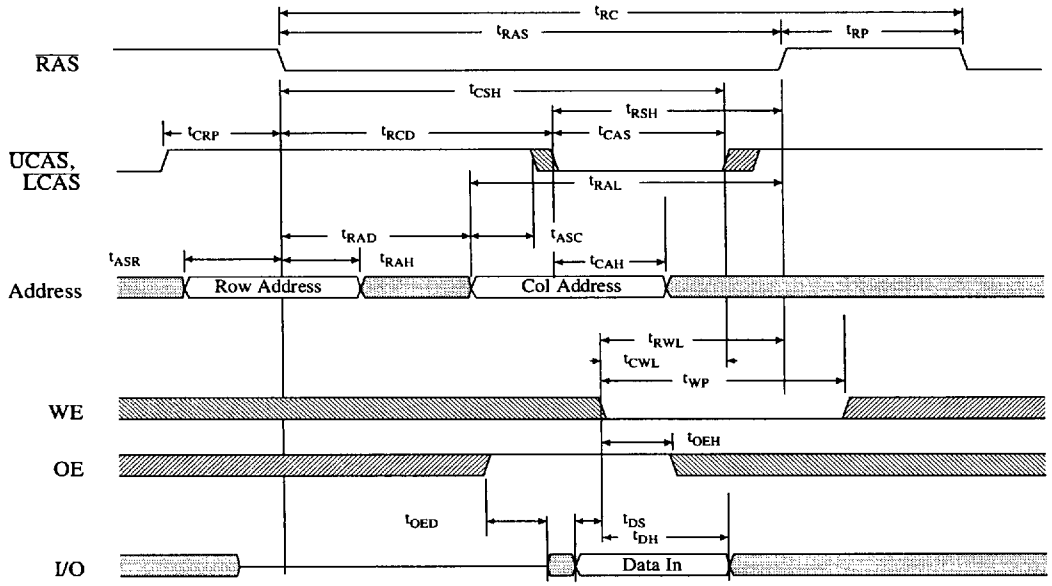
TIMING WAVEFORM OF UPPER BYTE EARLY WRITE CYCLE



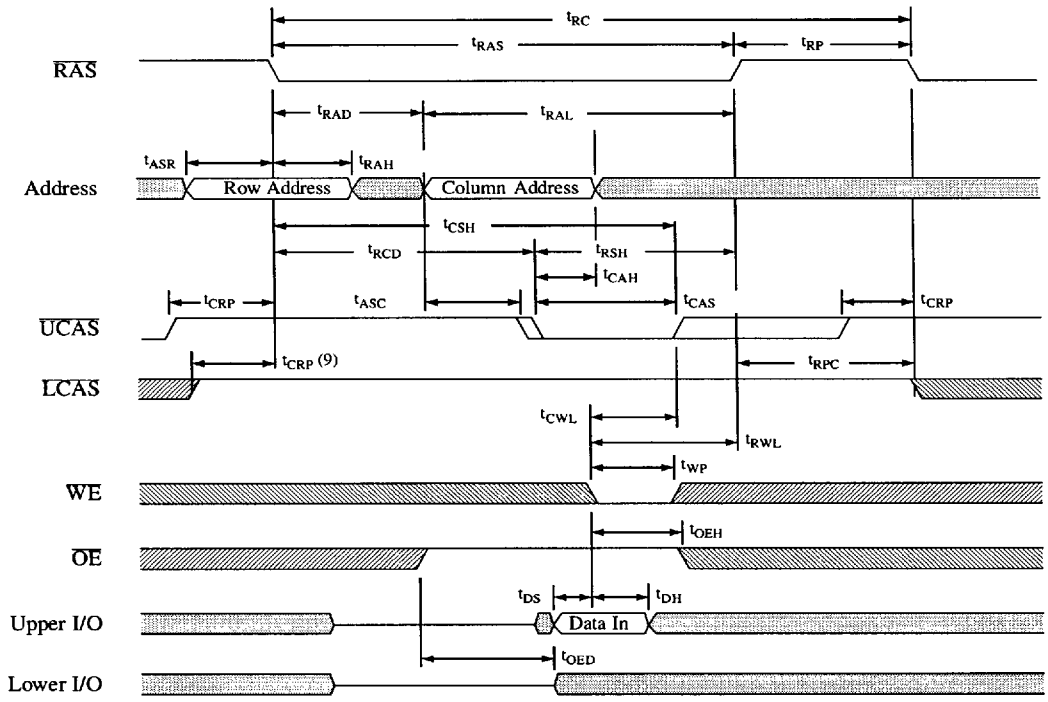
TIMING WAVEFORM OF LOWER BYTE EARLY WRITE CYCLE



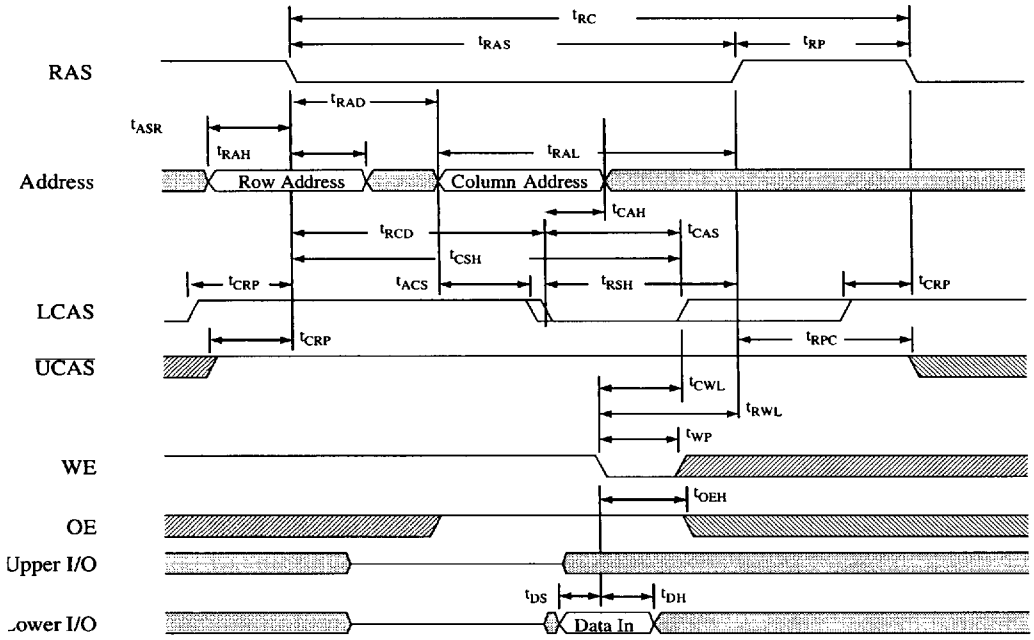
TIMING WAVEFORM OF WRITE CYCLE ($\overline{OE}$ Controlled)



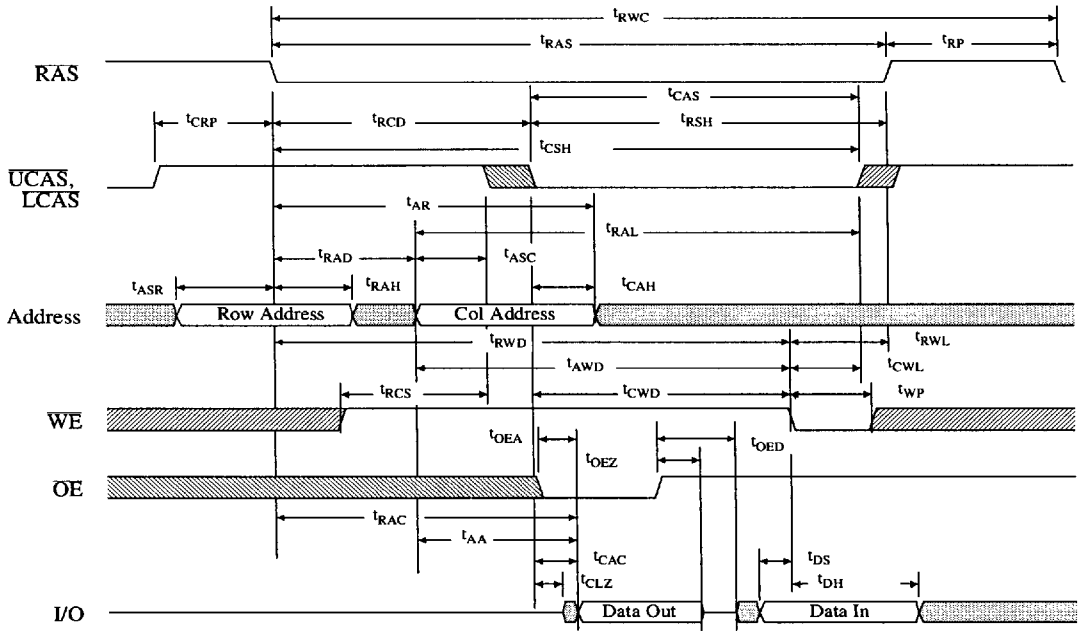
TIMING WAVEFORM OF UPPER BYTE WRITE CYCLE ($\overline{OE}$ Controlled)



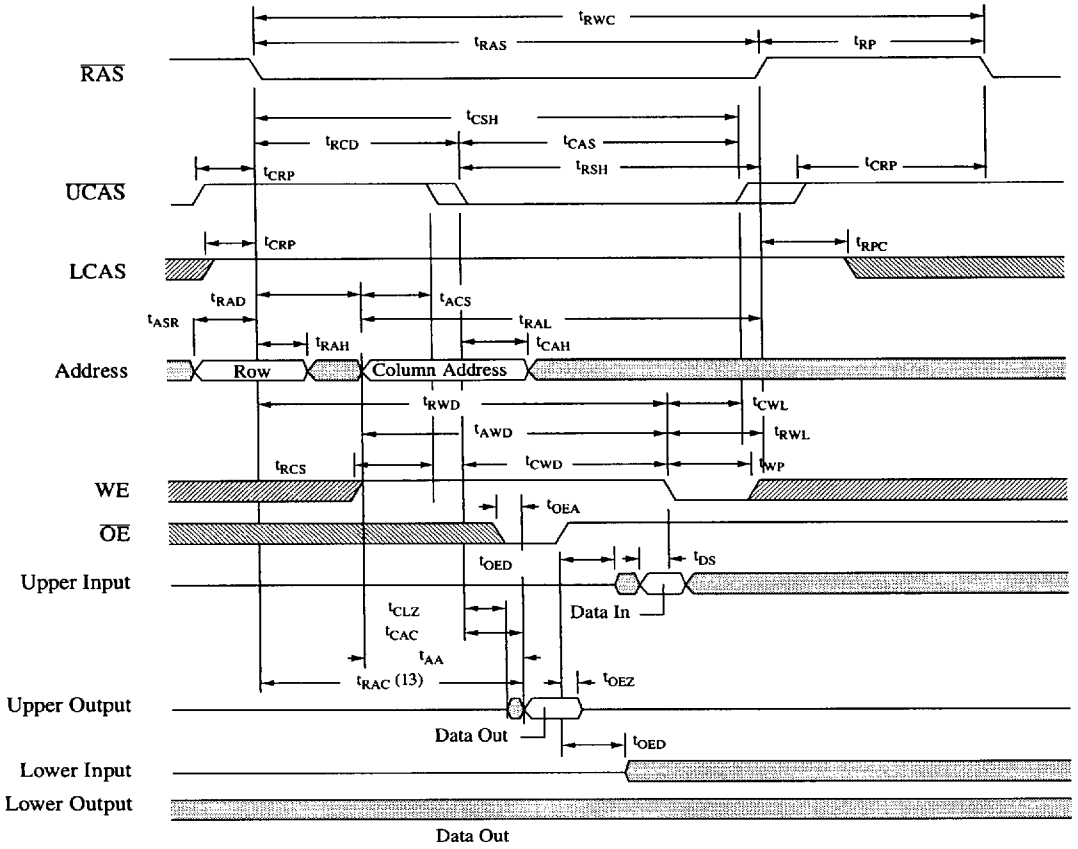
TIMING WAVEFORM OF LOWER BYTE WRITE CYCLE ($\overline{OE}$ Controlled)



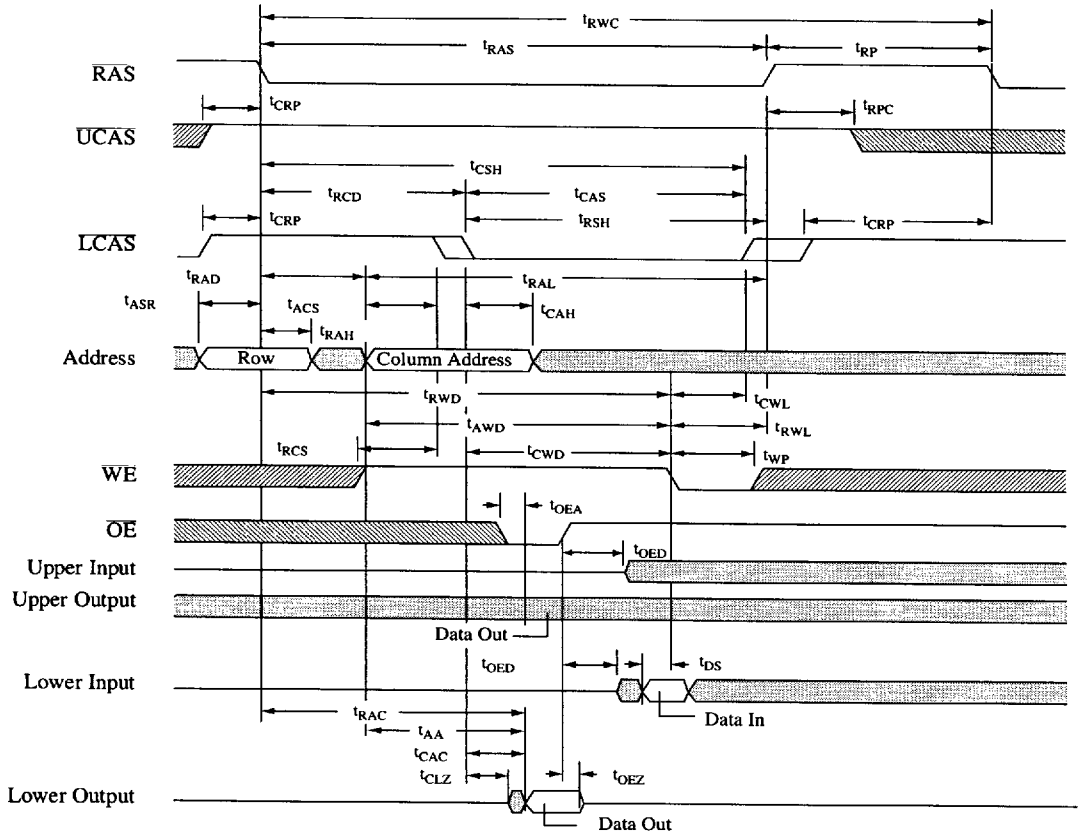
TIMING WAVEFORM OF READ-MODIFY-WRITE CYCLE



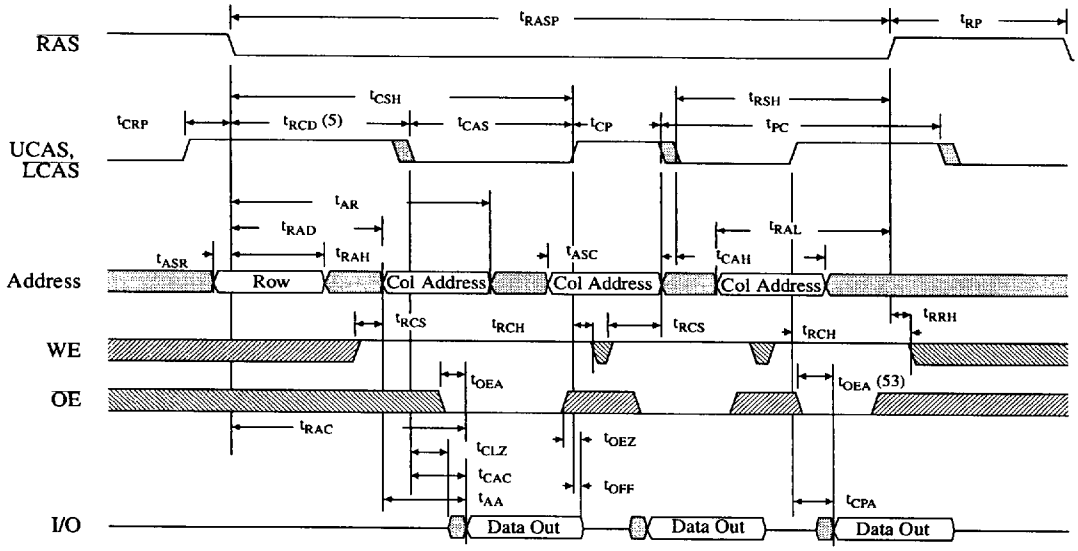
TIMING WAVEFORM OF UPPER BYTE READ-MODIFY-WRITE CYCLE



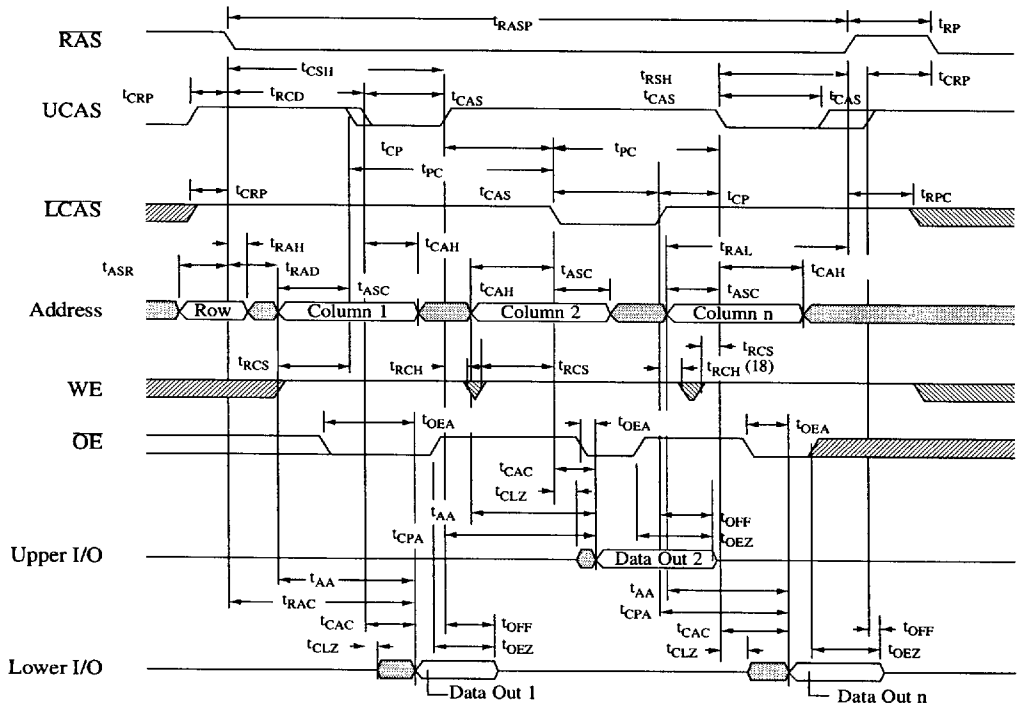
TIMING WAVEFORM OF LOWER BYTE READ-MODIFY-WRITE CYCLE



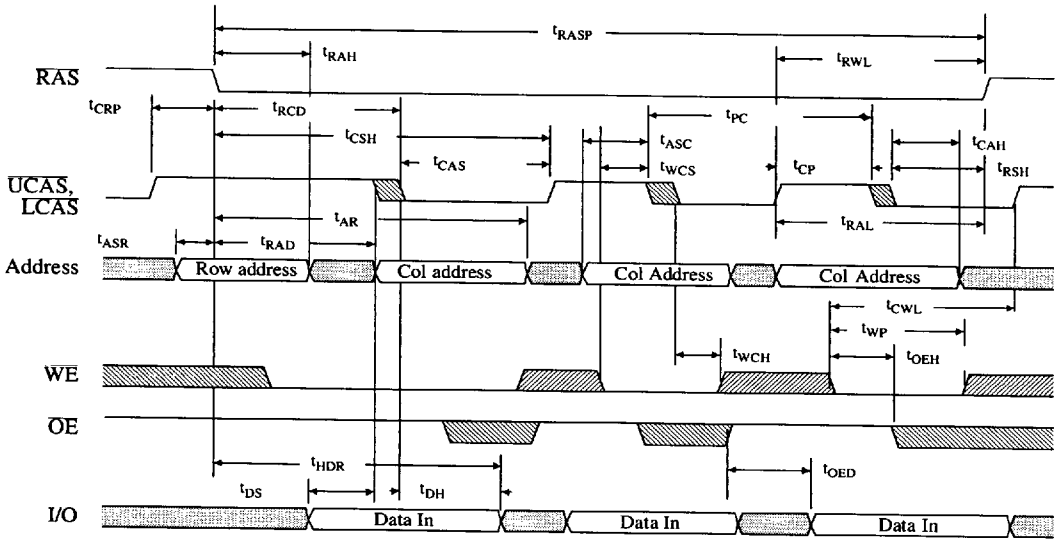
TIMING WAVEFORM OF FAST PAGE MODE READ CYCLE



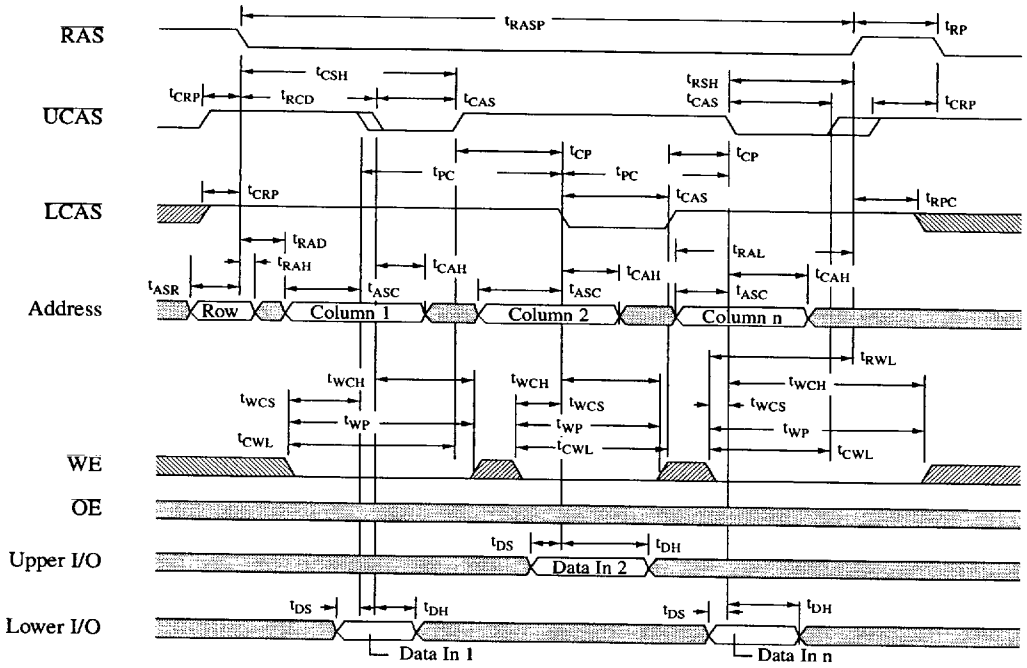
TIMING WAVEFORM OF FAST PAGE MODE BYTE READ CYCLE



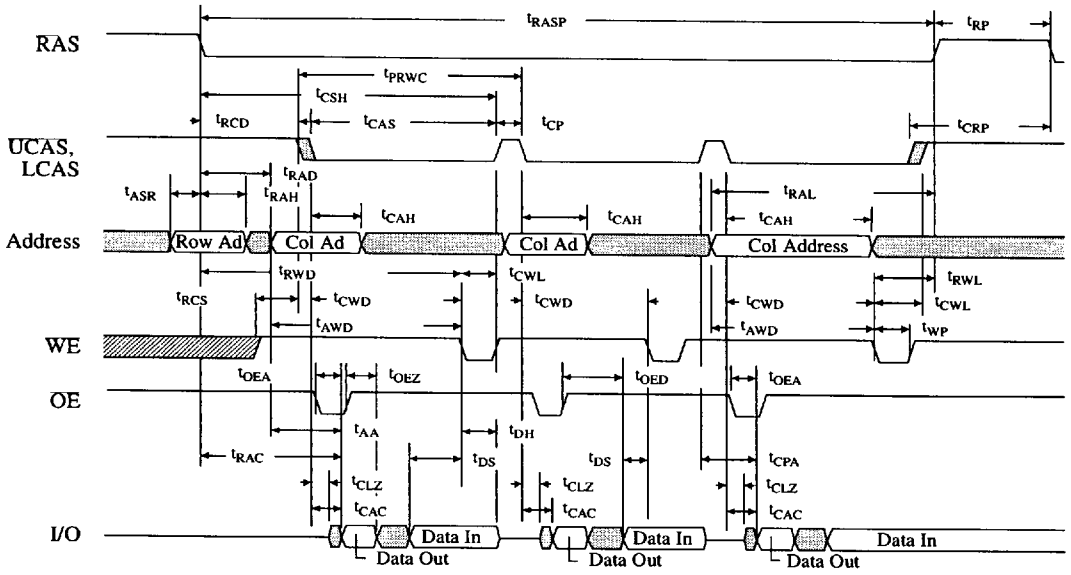
TIMING WAVEFORM OF FAST PAGE MODE EARLY WRITE CYCLE



TIMING WAVEFORM OF FAST PAGE MODE BYTE EARLY WRITE CYCLE

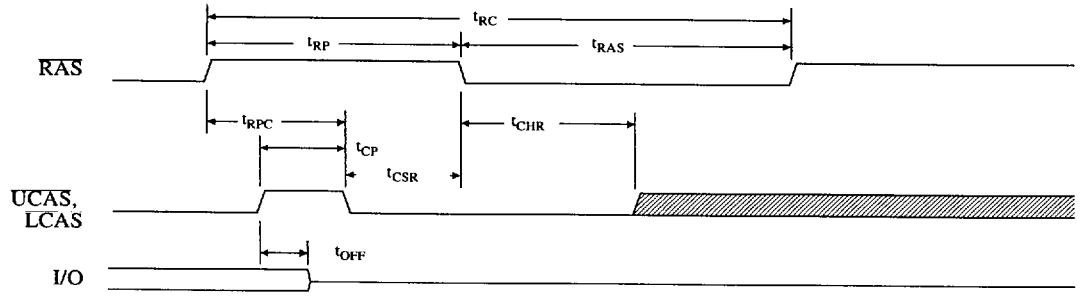


TIMING WAVEFORM OF FAST PAGE MODE READ-MODIFY-WRITE CYCLE



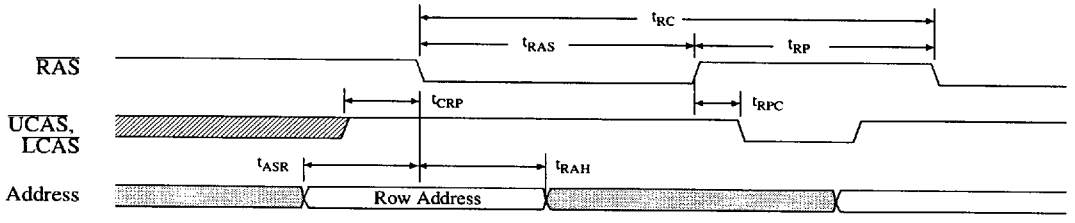
TIMING WAVEFORM OF $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

($\overline{WE}$ = A9 = V_{IH} or V_{IL})

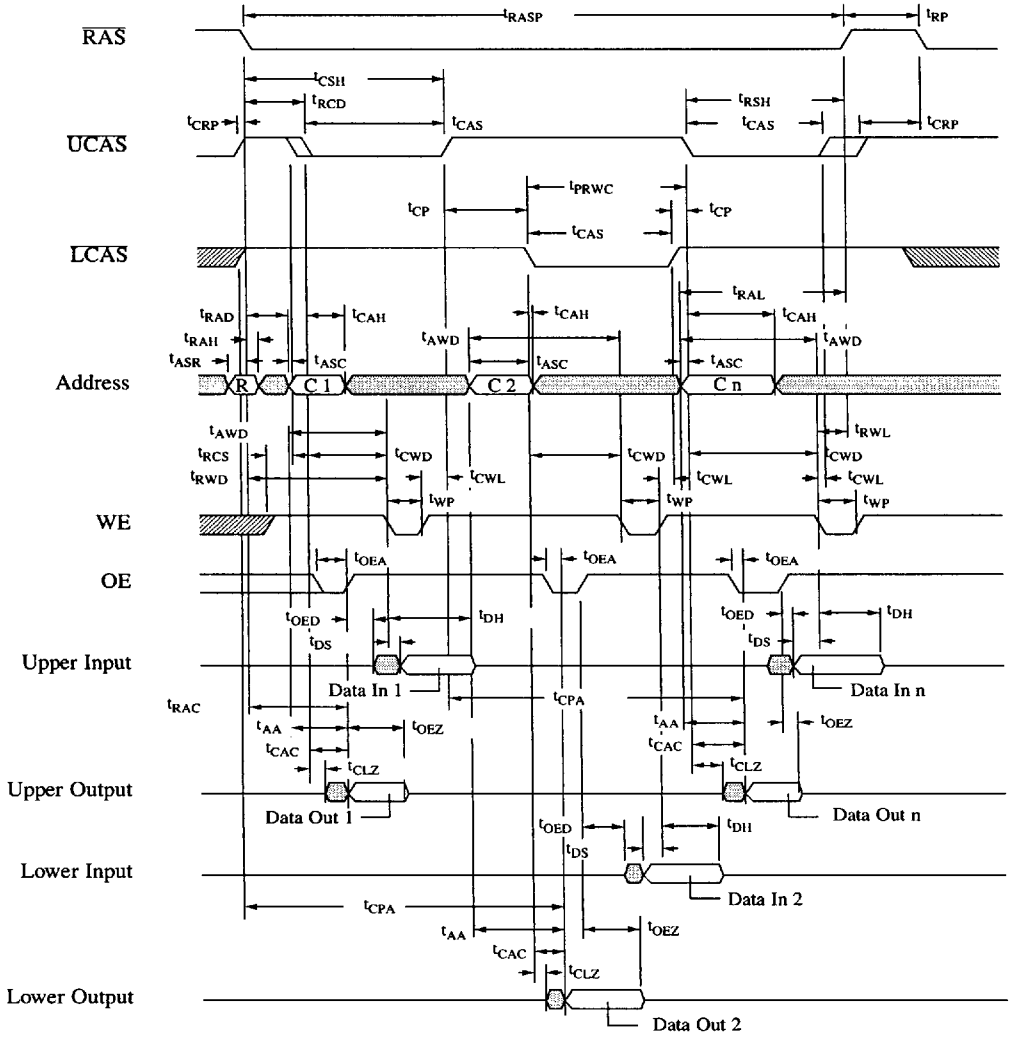


TIMING WAVEFORM OF $\overline{RAS}$ ONLY REFRESH CYCLE

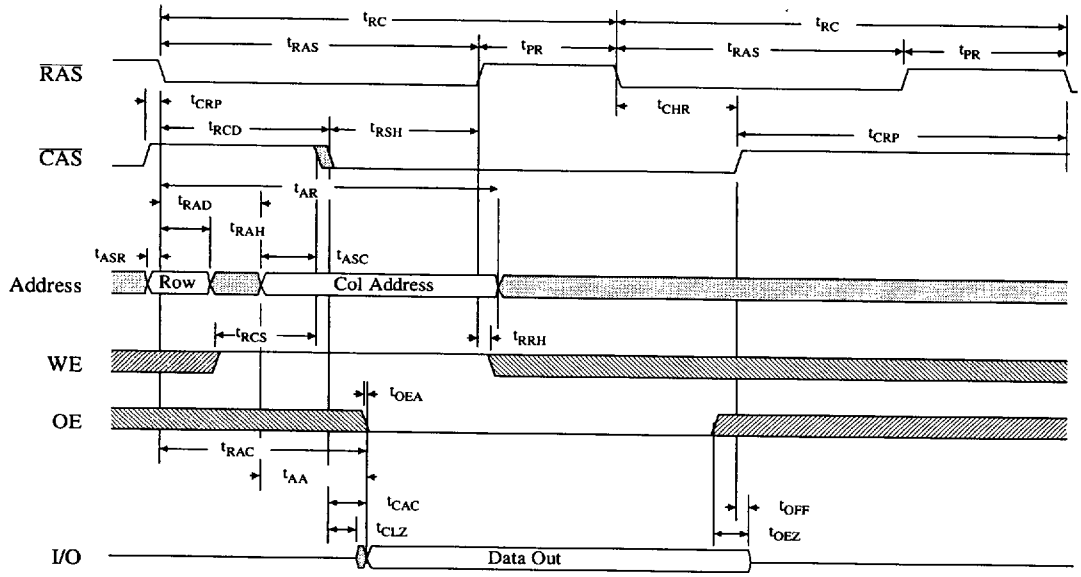
($\overline{WE}$ = $\overline{OE}$ = V_{IH} or V_{IL})



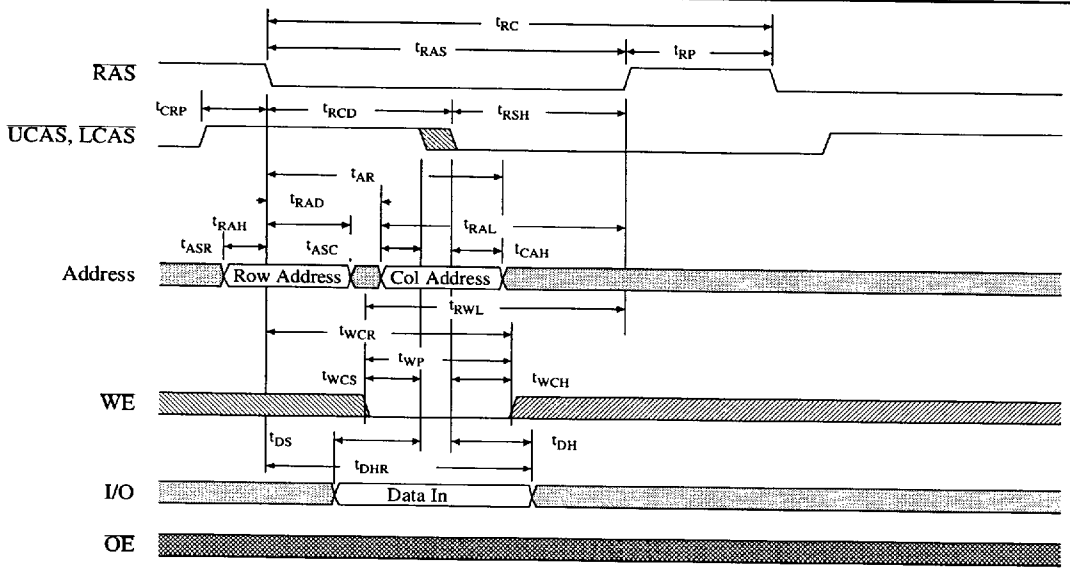
TIMING WAVEFORM OF FAST PAGE MODE BYTE READ-MODIFY-WRITE CYCLE



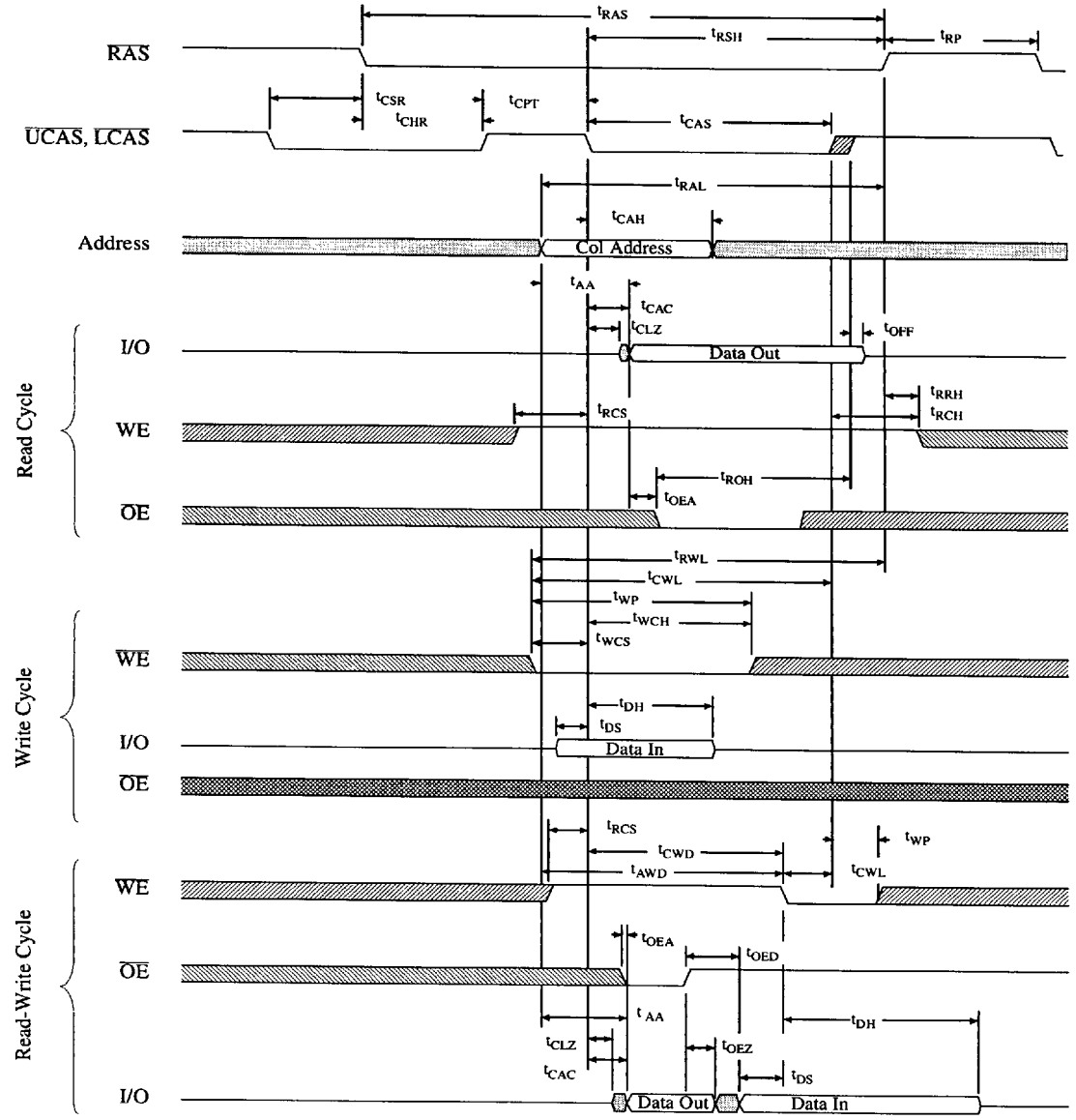
TIMING WAVEFORM OF HIDDEN REFRESH CYCLE (READ)



TIMING WAVEFORM OF HIDDEN REFRESH CYCLE (WRITE)



TIMING WAVEFORM OF $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



CAPACITANCE [15]

(f = 1 MHz, T_a = Room Temperature, V_{CC} = 5V±10%)

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input Capacitance	C_{IN1}	A0 to A8	V_{in} = 0V	5	pF
	C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	7	pF
I/O Capacitance	$C_{I/O}$	I/O0 to I/O15	V_{in} = V_{out} = 0V	7	pF

ORDERING CODES

Package \ $\overline{RAS}$ Access Time	50 ns	60 ns
Plastic SOJ, 400 mil, 40-pin	AS4C256K16F0-50JC	AS4C256K16F0-60JC

Shaded areas contain advance information.

PART NUMBERING SYSTEM

AS4C	256K16	F0	-XX	X	C
DRAM Prefix	Device Number	Fast Page Mode	$\overline{RAS}$ Access Time	Package: J = SOJ 400 mil	Commercial Temperature Range, 0°C to 70 °C